Protocol-Level Performance Analysis and Implementation for Anti-Collision Protocols in RFID Systems

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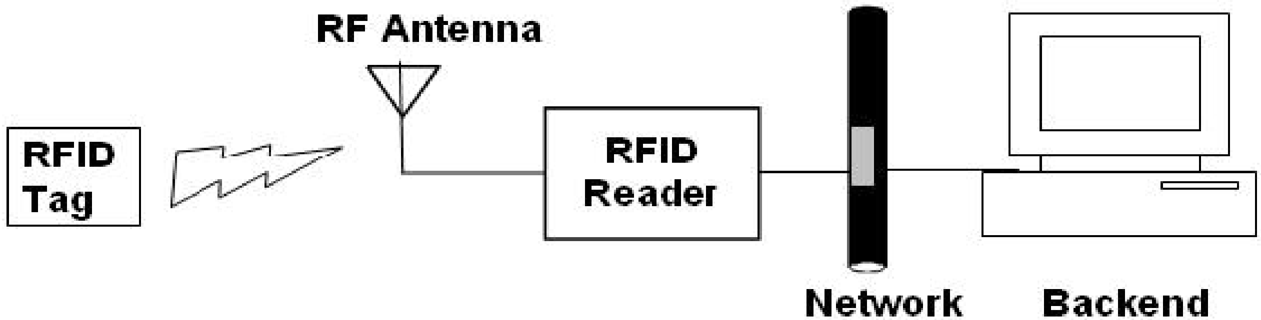
RFID System



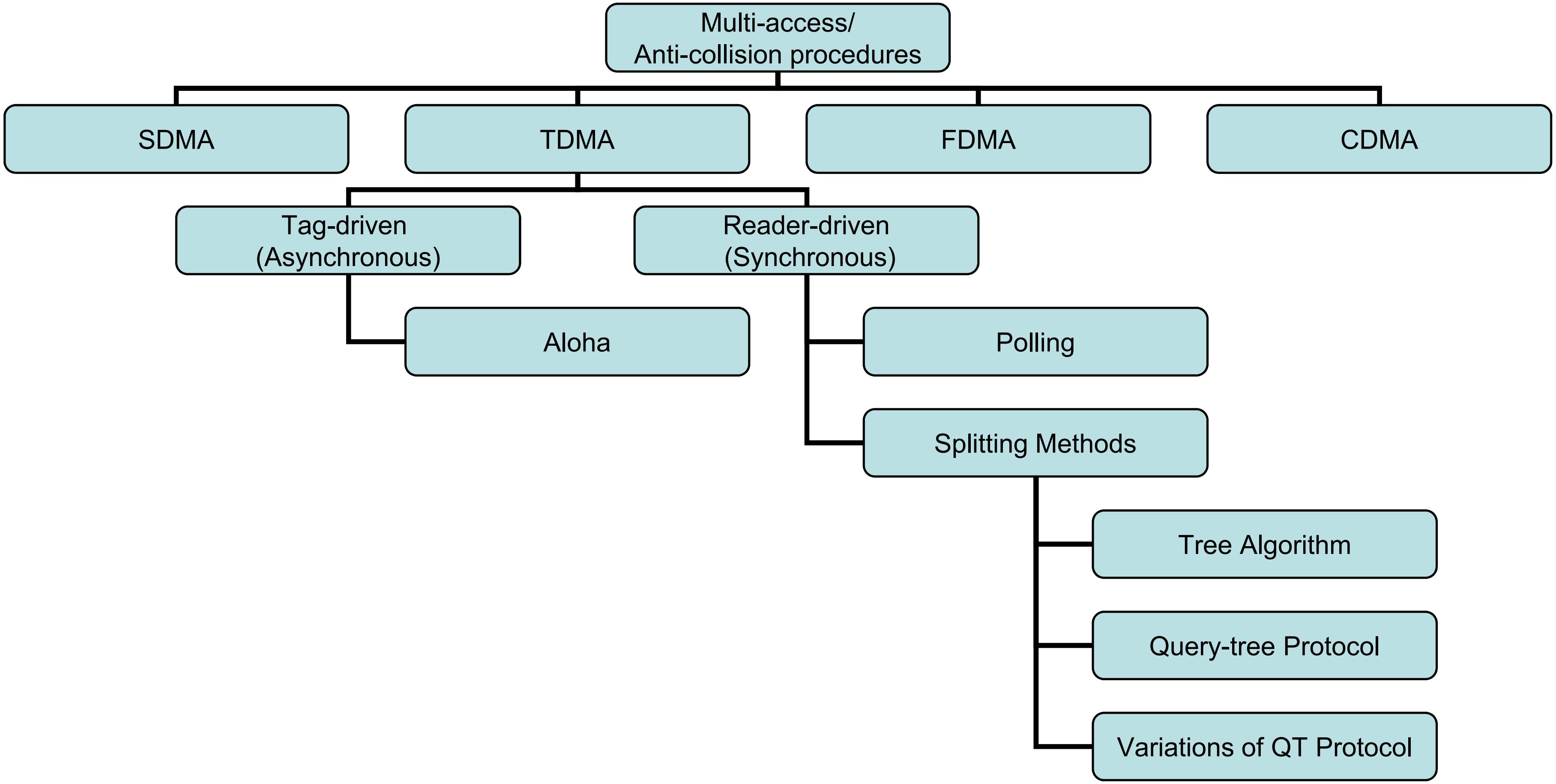
Problems with RFID Systems

- Problems with RFID systems
  - Tags might not be read due to collisions
- Types of collisions:
  - Single Reader-Multiple Tags interference
  - Single Tag-Multiple Readers interference
  - Reader-to-Reader interference

Single Reader-Multiple Tags interference

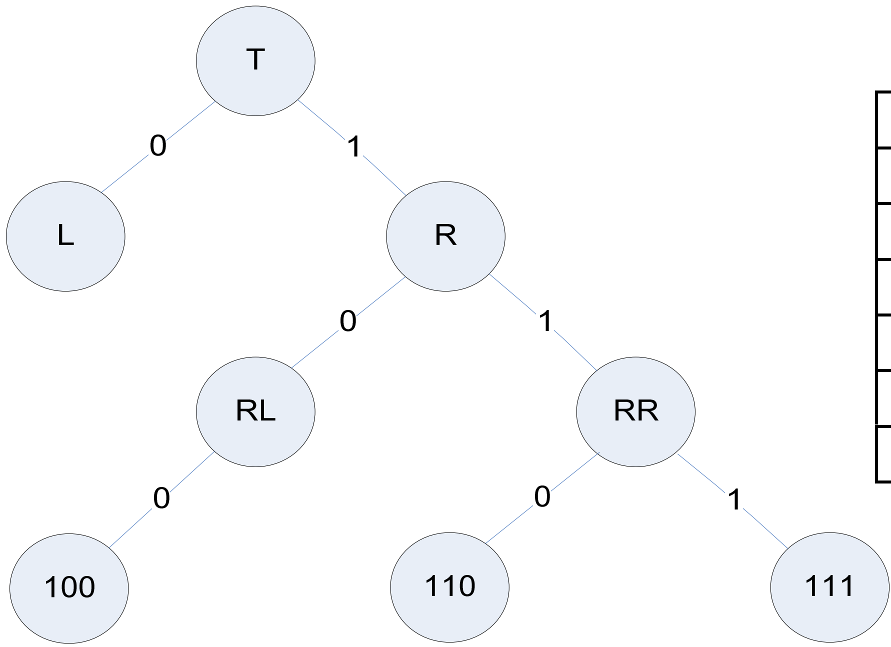
- Why countermeasures for tag collisions?
  - Library books, airline baggage, garment, and retail applications, etc.
- Resolution approach:
  - Need a systematic way of arbitration based on multiple access

Collision Resolution Protocols



Tree Algorithm

Reading tags with IDs: 100, 110, 111



Reader	Tag	Identified
0	No response	
1	*	
0	0	100
1	*	
0	0	110
1	1	111

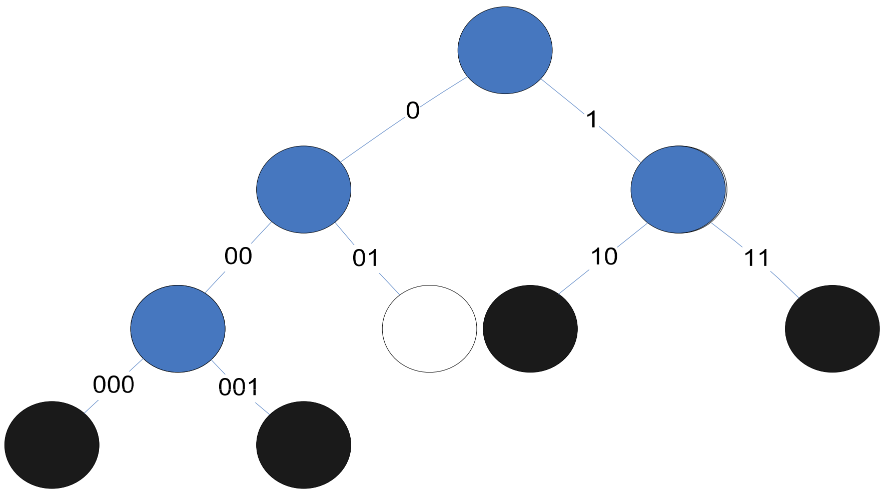
Search on a binary tree

Query Tree Algorithm

ID: {000, 001, 101, 110}

Step	1	2	3	4	5	6	7	8	9
Query	Null	0	1	00	01	10	11	000	001
Response	C	C	C	C	Z	S(101)	S(110)	S(000)	S(001)

c = collision, z = zero response, s = single response



Example of Query Tree

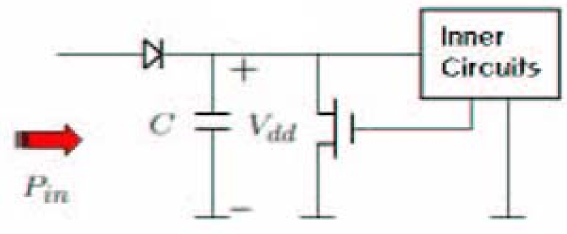
Related Work

Based on the literature:

- "Low Power Implementation of Anti-Collision Protocols for Radio-Frequency Identification Systems" by Feng Zhou and Chunghon Chen

Discusses:

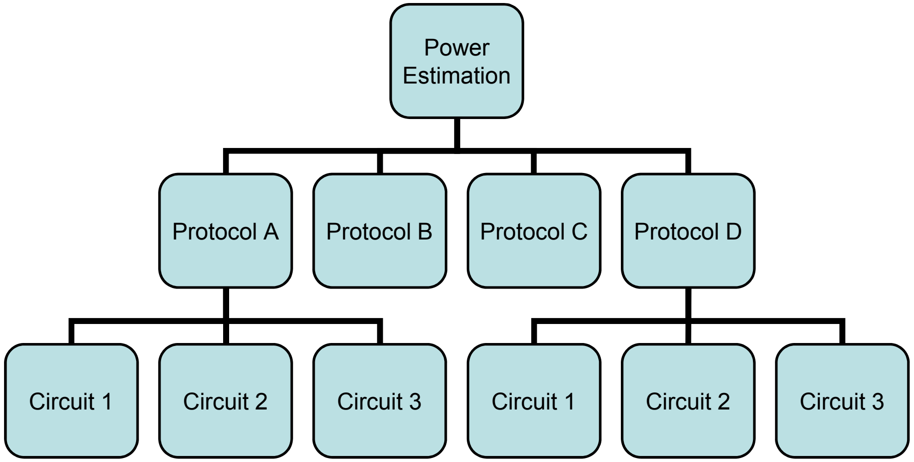
- Circuit level implementation of
  - Binary-Tree Protocol
  - Query-Tree Protocol
  - Improved Query-Tree Protocol
- Compares the three protocols in terms of power dissipation (Cost function):
- 1) Improved Query and Binary:
  - For R ≤ 14.4n – 274.2, COST $_{improved}$ ≤ COST $_{binary}$
- 2) Query and Binary:
  - For R ≤ 4n – 75, COST $_{query}$ ≤ COST $_{binary}$
- 3) Improved Query and Binary:
  - For R ≤ 153.96, COST $_{improved}$ ≤ COST $_{query}$



$$Where\ , R = \frac{C \cdot V_{drop}}{C_{load} \cdot V_{dd}}$$ and n is the ID length of a tag

Problem with the previous work and Motivation for this work

- Problem:
  - Circuit level power analysis bi-passing protocol level



- Motivation:
  - Power estimation is fast and inexpensive in protocol level

Work Done

- Formulated protocol level metric equations for different protocols
- Proposed a better protocol
- Performed evaluation of the protocols at protocol level
- Implemented the protocols
- Performed evaluation of the protocols at layout level

Protocol level power analysis

- Variables:
  - N = Total number of ID bits that represent a specific tag
  - n = number of tags that exit simultaneously for interrogation
  - T = number of transitions that a tag makes from state to state
  - Clk = total number of clock cycles a tag needs before read
- Condition:
  - Worst-case scenario
    - For any N and distribution of tags (n), the analysis will focus on the last tag to be read by the reader
- Metrics:
  - Optimize in terms of number of transitions, clock cycles, power consumption, and energy for best performance
  - Power dissipation considered to be directly proportional to the total number of transitions
  - Energy dissipation evaluated as total number of transitions per total clock cycles

Protocol level power analysis

- Binary Protocol

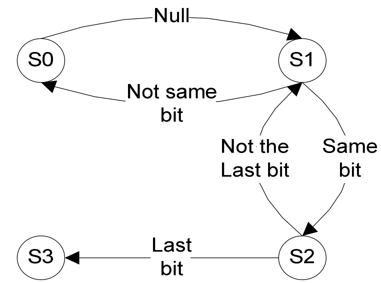


Fig. 1. State diagram

Total number of clock cycles (CLK_B) and total transitions (T_B) for any N and n, under worst case scenario:

- For $2 \le n \le 2^{N-2}$,

$$CLK_B = 3 + n(2N - 1) \quad (1)$$

$$T_B = T_{0-1} + T_{1-0} + T_{1-2} + T_{2-1} + T_{2-3} \quad (2)$$

$$T_B = 2 + \left(n - 2^l\right) \times 2(N - l - 1) + \sum_{j=1}^{l} \left[2^j (N - j)\right] + 2N - 1$$

$$= 2^{(l+2)} + 2n(N - l - 1) - 1 \quad (3)$$

- For $2^{N-2} \le n \le 2^{N-1}$,

$$CLK_B = n(2N - 1) \quad (4)$$

$$T_B = 2\left(n - 2^l\right) + 2N - 1 + \sum_{j=1}^{l} \left[2^j (N - j)\right]$$

$$= 2^{(l+1)}(N - l) + 2n - 3 \quad (5)$$

where

$$l = \lceil \log_2 n \rceil - 1 \quad (6)$$

Table 1. Identification Process of Two Tags by Binary-Tree Protocol for $N = 4$

Reader	*PS*	T_{0-1}	T_{1-0}	T_{1-2}	T_{2-1}	T_{2-3}	*Clk*	*NS*	*Tag*
Null	S0	1					1	S1	
0	S1		1				1	S0	
	S0						1	S0	No Response
Reset	S0	1					1	S1	
1	S1			1			1	S2	
	S2				1		1	S1	
1	S1			1			1	S2	
	S2				1		1	S1	
0	S1		1				1	S2, S0	
	S2						1	S3	#12
Reset	S0	1					1	S1	
1	S1			1			1	S2	
	S2				1		1	S1	
1	S1			1			1	S2	
	S2				1		1	S1	
1	S1			1			1	S2	
	S2					1	1	S3	#14
Total	-	3	2	5	4	1	17	-	-

Protocol level power analysis

- Query Protocol

Total number of clock cycles (CLK_Q) and total transitions (T_Q) for any N and n, under worst case scenario:

$$T_Q = T_{0-1} + T_{1-0} + T_{1-2} + T_{2-0}$$
$$= T_{QT}(n, N) - T_{1-1} - T_{2-2} \qquad (7)$$

where $T_{QT}(n, N)$ is total state transitions including the self-loops (T_{1-1} and T_{2-2}) .

- For $2 \leq n \leq 2^{N-1}$,

$$CLK_Q = (2n-1)(N+2) \qquad (8)$$

$$T_{QT}(n, N) = \left[2\left(n-2^{l}\right)-1\right](N-l) + 2^{(l+1)}(N-l+2) + \frac{l^2+3l}{2} \qquad (9)$$

$$T_{1-1} = 2n(N-l-2) + 2^{(l+2)} - 2N + l + 1 \qquad (10)$$

$$T_{2-2} = (N-1) + \sum_{j=1}^{l} j = (N-1) + l\left(\frac{l+1}{2}\right) \qquad (11)$$

$$T_Q = T_{QT} - T_{1-1} - T_{2-2} = l + 4n \qquad (12)$$

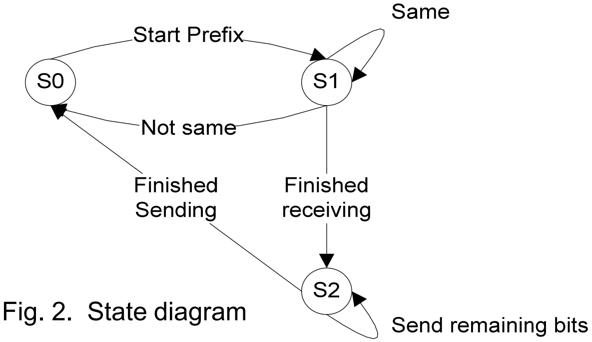


Fig. 2. State diagram

Table 2. Identification Process of Two Tags by Query-Tree Protocol for $N = 5$

Reader	PS	$T_{0\text{-}1}$	$T_{1\text{-}0}$	$T_{1\text{-}1}$	$T_{1\text{-}2}$	$T_{2\text{-}0}$	$T_{2\text{-}2}$	Clk	NS	Tag
Null	S0	1						1	S1	
Null	S1							1	S2	
	4* S2						4	4	4* S2	
	S2					1		1	S0	
Null	S0	1						1	S2	
1	S1			1				1	S1	
1	S1			1				1	S1	
1	S1			1				1	S1	
0	S1		1					1	S1, S0	
Null	S1							1	S2	
	S2							1	S0	#28
Null	S0	1						1	S1	
1	S1			1				1	S2	
1	S1			1				1	S1	
1	S1			1				1	S1	
1	S1			1				1	S2	
Null	S1				1			1	S1	
	S2					1		1	S3	#30
Total	-	3	1	7	2	2	4	21	-	-

Protocol level power analysis

- Improved Query Protocol

Same as Query-Tree Protocol except the 'Stop-Send' command during collision

- For $2 \le n \le 2^{N-1}$,

→ total transitions (T_{IQ}) = (T_Q)

$$T_{IQ} = T_Q = l + 4n \qquad (13)$$

Total number of clock cycles (CLK_{IQ})

$$CLK_{IQ} = \left\{ \sum_{j=0}^{l-1} \left[\left(\mathrm{int}\left(\frac{n - 2^{(j+1)} - 1}{2^{(j+2)}} \right) + 1 \right) (N + 1 - j) \right] + (N+2)[1 + n + k] \right\} \qquad (14)$$

$$where, \qquad k = \left\lceil \frac{n-3}{2} \right\rceil$$

- As a special case, if $n = 2^m$, then

$$CLK_{IQ}(n = 2^m) = 2^{(m-1)}(4N + 6) + (m - N - 1) \qquad (15)$$

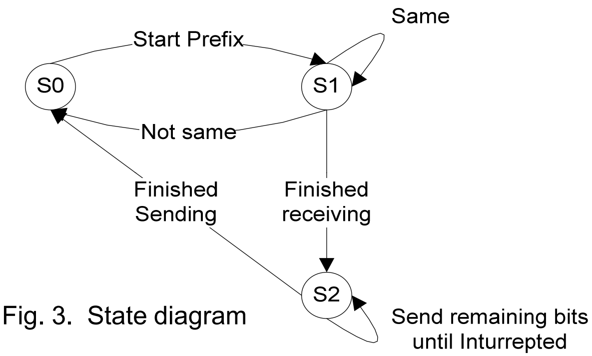


Fig. 3. State diagram

Table 3. Identification Process of Two Tags by Improved Query-Tree Protocol for $N = 5$

Reader	*PS*	$T_{0\text{-}1}$	$T_{1\text{-}0}$	$T_{1\text{-}1}$	$T_{1\text{-}2}$	$T_{2\text{-}0}$	$T_{2\text{-}2}$	*Clk*	*NS*	*Tag*
Null	S0	1						1	S1	
Null	S1				1			1	S2	
	4* S2						4	4* S2	S2	
SS	S2					1		1	S0	
Null	S0	1						1	S2	
1	S1			1				1	S1	
1	S1			1				1	S1	
1	S1			1				1	S1	
0	S1		1					1	S1, S0	
Null	S1							1	S2	
	S2							1	S0	#28
Null	S0	1						1	S1	
1	S1			1				1	S1	
1	S1			1				1	S1	
1	S1			1				1	S1	
1	S1			1				1	S1	
Null	S1				1			1	S2	
	S2					1		1	S0	#30
Total	-	3	1	7	2	2	4	21	-	-

Protocol level power analysis

- The Proposed Protocol
  - combines binary-tree and query-tree protocols

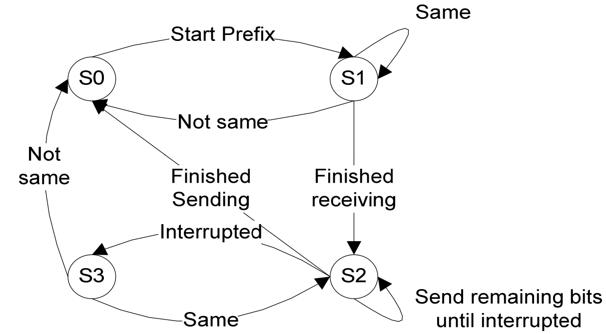


Fig. 4. State diagram

Total number of clock cycles (CLK_{BQ}) and total transitions (T_{BQ}) derivation, under worst case scenario:

$$T_{BQ} = T_{BQT} - T_{1-1} - T_{2-2} \qquad (16)$$

- For $2 \leq n \leq 2^{N-1}$,

$$CLK_{BQ} = n(N+3) - 1 \qquad (17)$$

$$T_{BQT} = 2^{(l+1)} + l(2-n) + Nn + 2 \qquad (18)$$

$$T_{1-1} = n(N-l-2) + 2^{(l+1)} - N + l + 1 \qquad (19)$$

$$T_{2-2} = (N-l) - 2 \qquad (20)$$

$$T_{BQ} = T_{BQT} - T_{1-1} - T_{2-2} = 2(l+n) + 3 \qquad (21)$$

Table 4. Identification Process of Two Tags by Combined Binary Query-Tree Protocol for $N = 5$

Reader	PS	T_{0-1}	T_{1-0}	T_{1-1}	T_{1-2}	T_{2-0}	T_{2-2}	T_{2-3}	T_{3-2}	T_{3-0}	Clk	NS	Tag
Null	S0	1									1	S1	
Null	S1				1						1	S2	
	S2						3				3	S2	
SS	S2							1			1	S3	
0	S3									1	1	S0,S2	
	S2										1	S0	#28
Null	S0	1									1	S1	
1	S1			1							1	S0,S1	
1	S1			1							1	S0,S1	
1	S1			1							1	S0,S1	
1	S1			1							1	S0,S1	
Null	S1				1						1	S2	
	S2					1					1	S0	#30
Total		2	0	4	2	1	3	1	0	1	15		

Protocol-level Performance Evaluation of different protocols

- The performance of Binary, Query, and Improved-Query tree protocols is evaluated in terms of
  - total number of state transitions, number of clock cycles, energy and power dissipation, all under their worst cases
- Number of state transitions is a key metric for estimation of power and energy dissipation
- Number of clock cycles determines how fast the tags can be identified
- For fair power dissipation comparison, the three protocols need to have same latency
  - i.e. protocol with less clock cycles can use a lower clock frequency to achieve power reduction
- Choosing the Improved-Query-tree protocol as a reference, equivalent transitions are:

$$\left.\begin{aligned} T_{B,eq} &= T_B\left(\frac{CLK_B}{CLK_{IQ}}\right) \\ T_{Q,eq} &= T_Q\left(\frac{CLK_Q}{CLK_{IQ}}\right) \\ T_{IQ,eq} &= T_{IQ} \end{aligned}\right\} \qquad (22)$$

Where $T_{B\,eq}$ and $T_{Q\,eq}$ are the equivalent number of state transitions for Binary and Query protocols respectively

Comparison of the three tree-based protocols

- Comparison of the above three protocols is shown in the following figure
  - it is plotted using the equations derived and assuming *n* = 4.

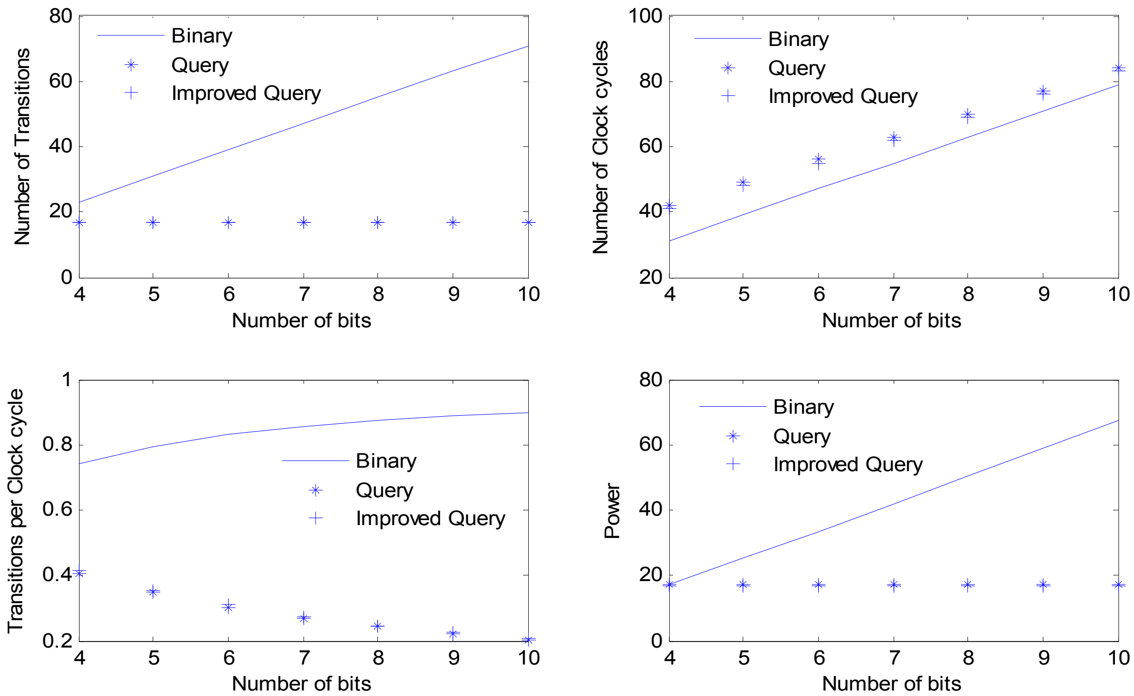


Fig. 5. Performance comparison of binary-tree, query-tree and Improved-query-tree protocols under their worst cases.

Comparison of protocols with the Proposed Protocol

- Comparison of The proposed protocol with others is shown in the following figure
  - it is plotted with $n = 4$.

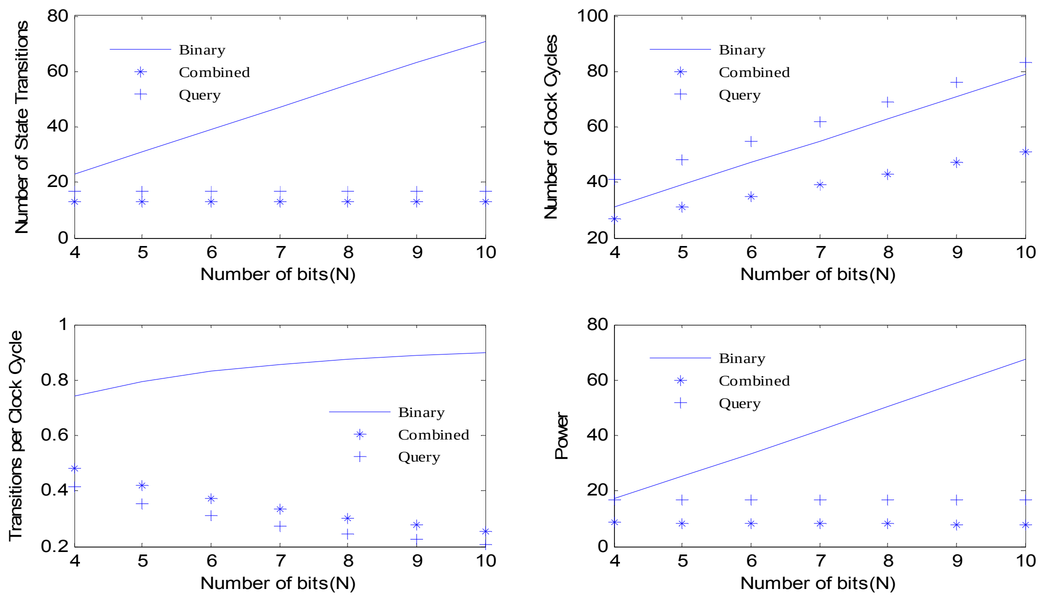


Fig. 6. Performance comparison of binary-tree, query-tree and combined binary-query-tree protocols under their worst cases.

- From the figure
  - the proposed protocol outperforms other two protocols in terms of number of transitions, number of clock cycles and power.
  - from the energy dissipation point of view, the query-tree protocol shows the best performance.

Implementation of protocols and Layout-level Performance Evaluation

- All protocols are implemented with the following information:
  - N = 4, n = 4, and for the worst case tag (tag # 15)
  - Verilog code was designed using Verilog-XL from Cadence
  - Simulation was performed using SimVision from Cadence
  - Gate level synthesis using design_vision from Synopsys
  - Layout using Encounter and Virtuoso from Cadence
- A) Binary Protocol

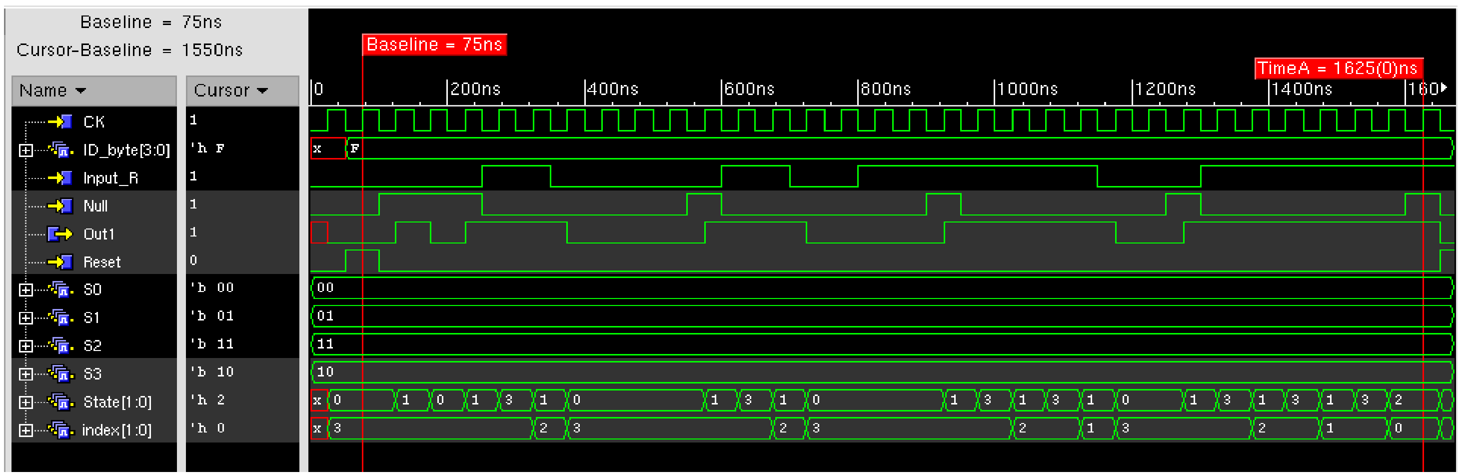


Fig. 7. Simulation output for Tag # 15, N = 4, n = 4: Binary-Tree Protocol.

A) Binary Protocol

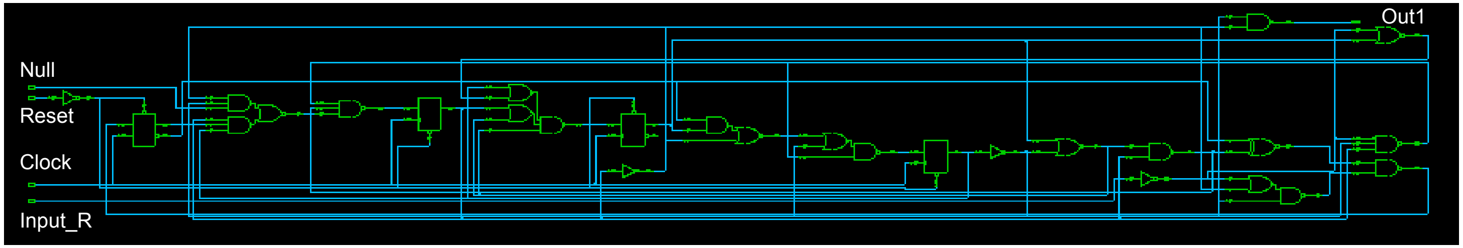


Fig. 8. Schematic for Tag # 15, N = 4: Binary-Tree Protocol

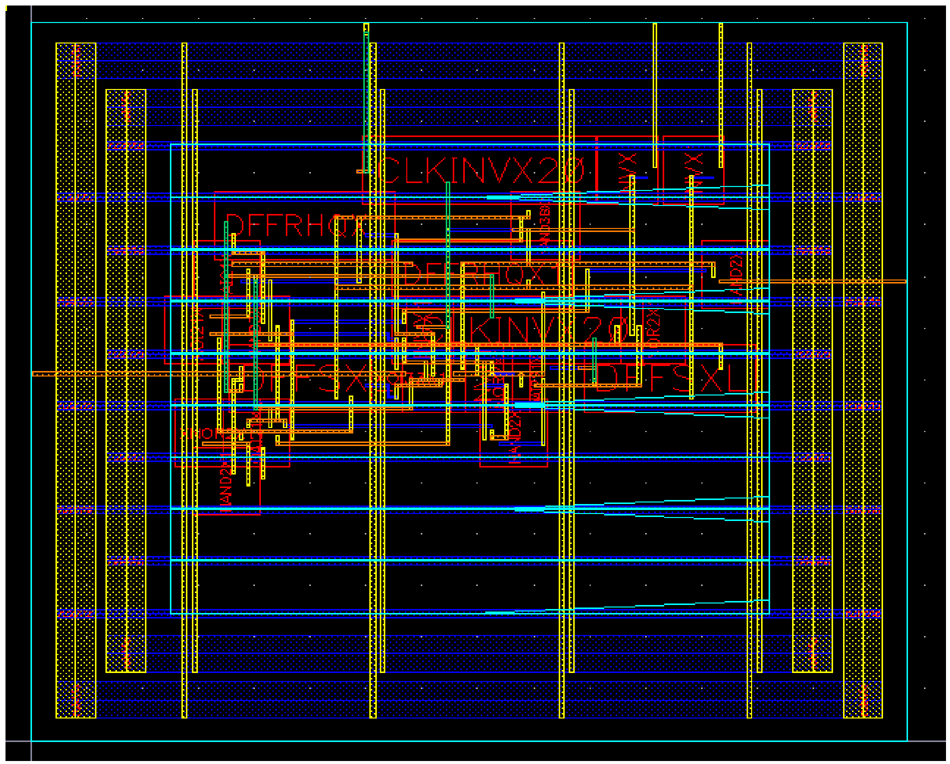


Fig. 9. Layout for Tag # 15, N = 4: Binary-Tree Protocol

Implementation of Query protocol

B) Query-Tree Protocol

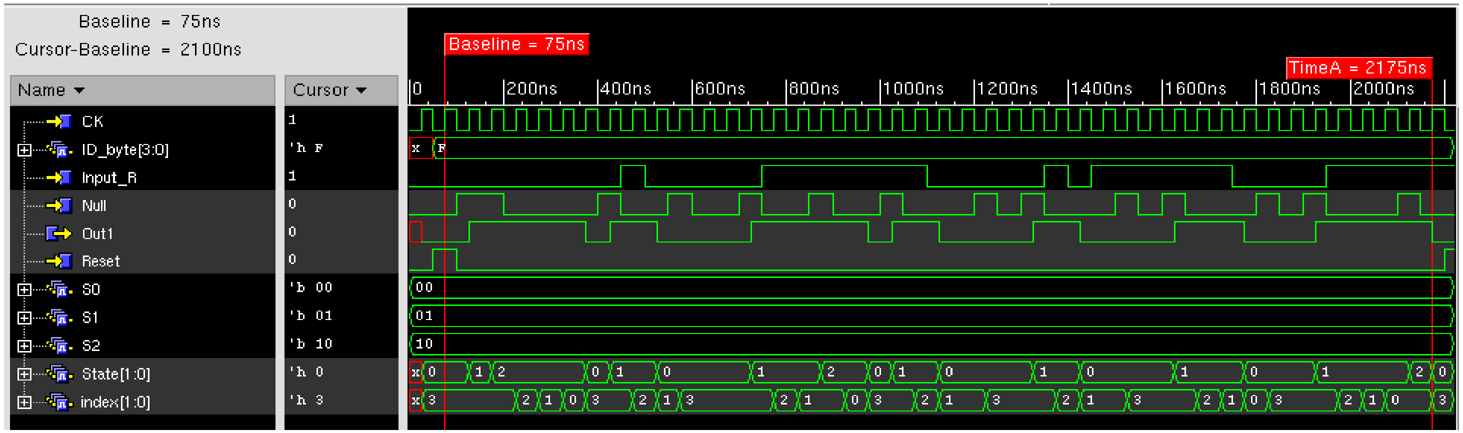


Fig. 10. Simulation output for Tag # 15, N = 4, n = 4: Query-Tree Protocol.

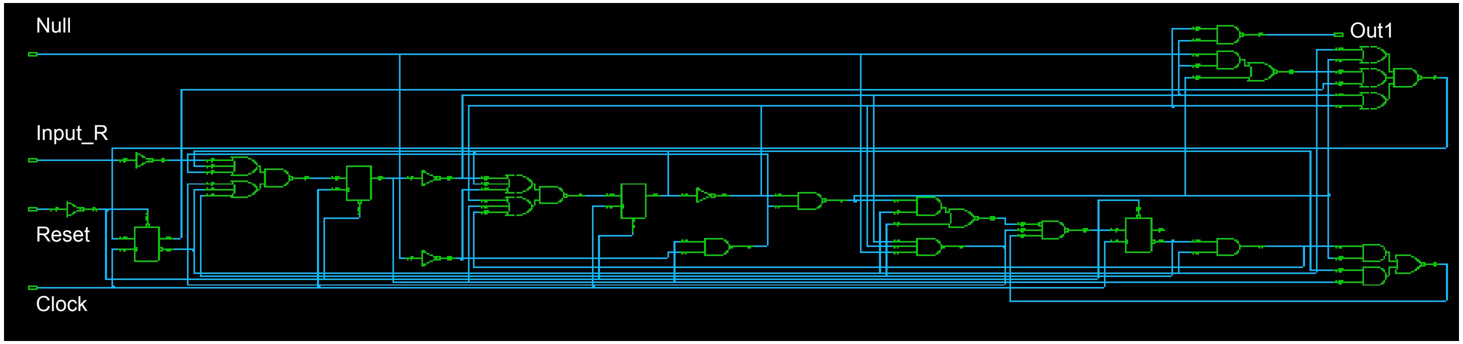


Fig. 11. Schematic for Tag # 15, N = 4: Query-Tree Protocol.

Implementation of Improved-Query protocol

C) Improved-Query-Tree Protocol

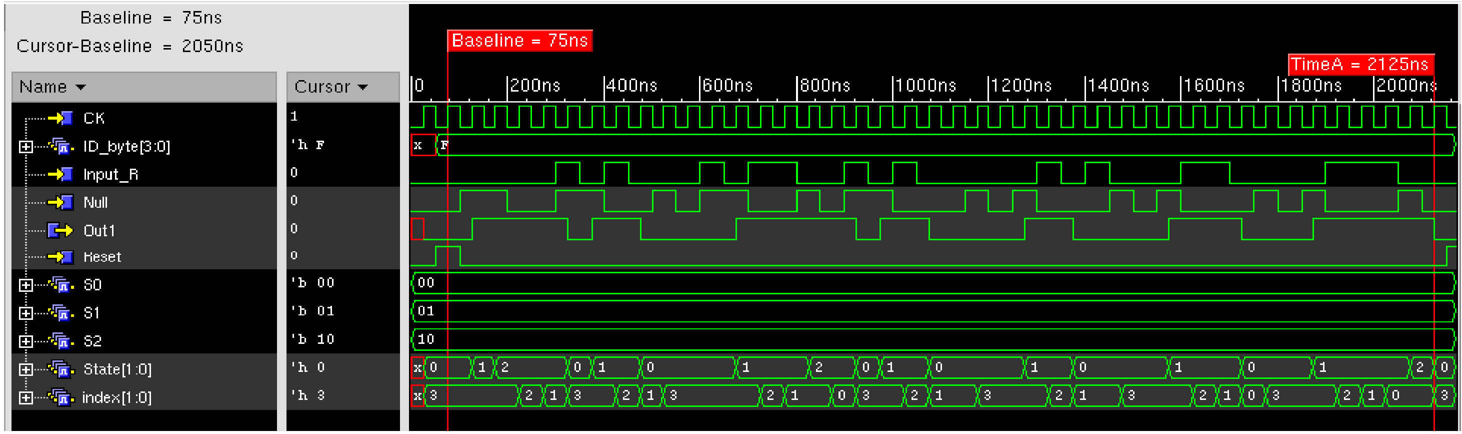


Fig. 12. Simulation output for Tag # 15, N = 4, n = 4: Improved-Query-Tree Protocol.

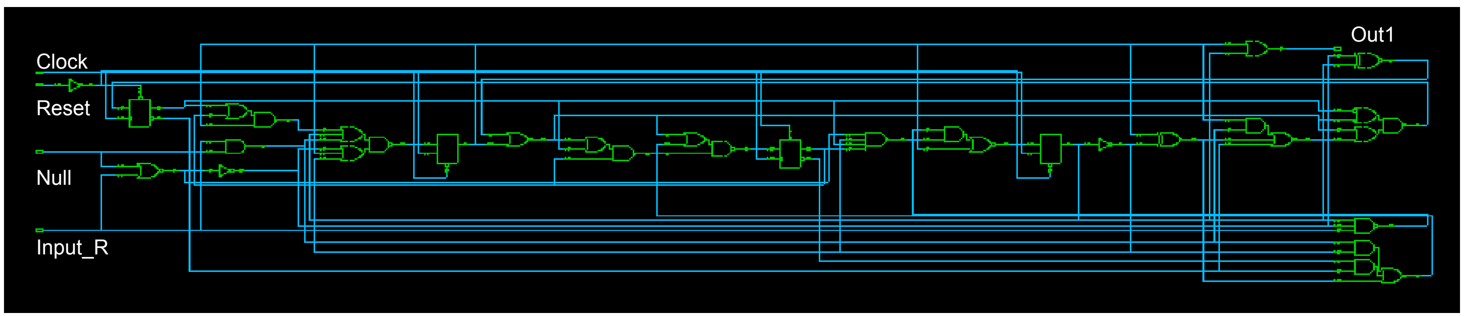


Fig. 13. Schematic for Tag # 15, N = 4: Query-Tree Protocol.

Implementation of the Proposed protocol

D) Combined-Binary-Query-Tree Protocol

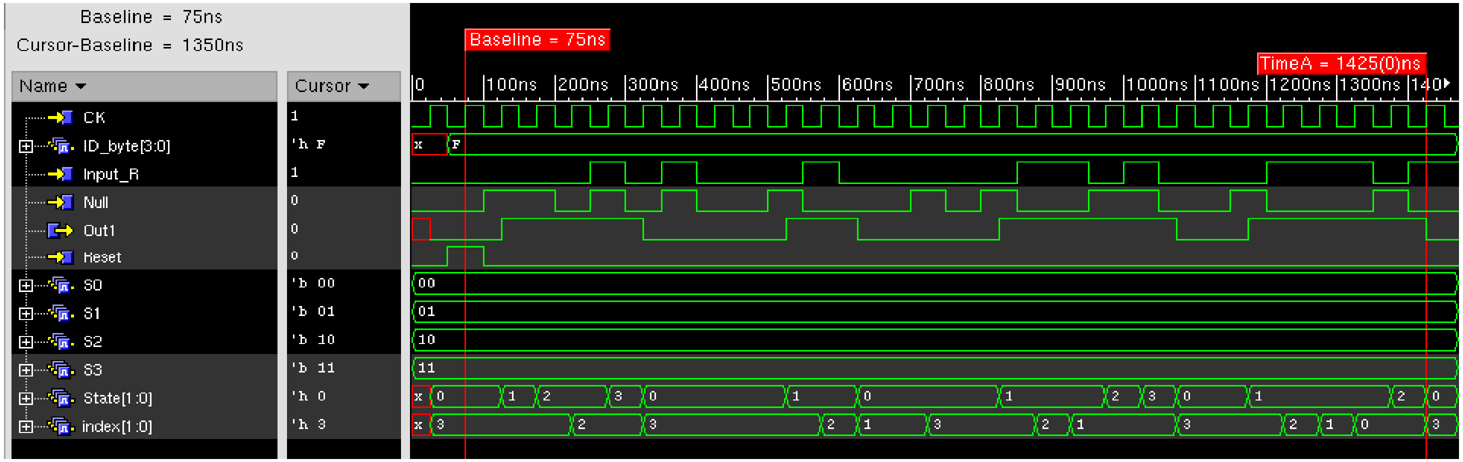


Fig. 14. Simulation output for Tag # 15, N = 4, n = 4: Combined-Binary-Query-Tree Protocol.

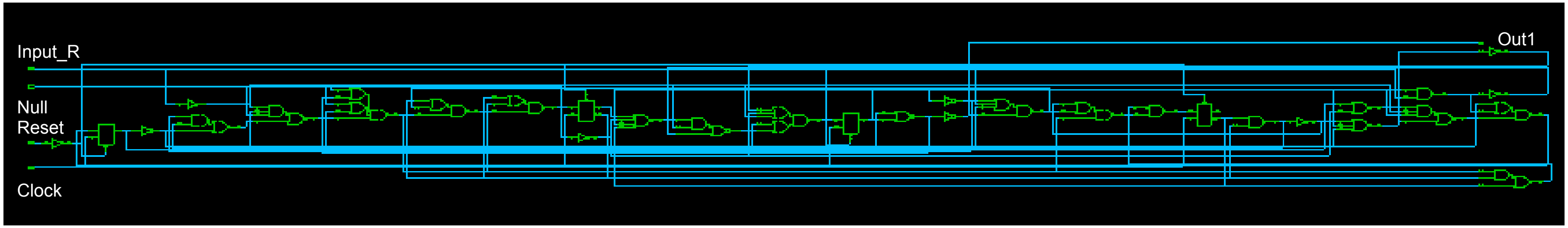


Fig. 15. Schematic for Tag # 15, N = 4: Combined-Binary-Query-Tree Protocol.

Layout-level Performance Evaluation of the four protocols

For each protocol:

- number of clock cycles is calculated from the simulation output
  - Clock Cycles = Total read time * 20MHz
- Power dissipation is determined using
  - Total switching activity by generating a VCD file
  - Total capacitance obtained from the layout level
  - Supply voltage = 1.62V
  - Frequency of operation = 20MHz
- General Power Equations are:

$$P_{sw} = 0.5 * C_{load} * V_{dd}^{2} * f_{clk} * E(transition\ s)$$
$$where, \quad C_{load} = \sum_{allfanout} C_G^{\,i} + C_{wire} \qquad (23)$$

$$P_{\text{int}} = 0.5 * V_{dd}^{2} * f_{clk} * \sum_{i=1}^{N} \left[C_G^{\,i} * E^{i}(transition\ s) \right] \qquad (24)$$

- P_{sw} and P_{int} are switching and internal powers, N_{in} is # of internal nodes,
- C_G^i is gate capacitance of i^{th} fanout and C_{wire} is interconnect capacitance of the driver net
- E^i(transitions) is expected # of transitions at node i.

Layout-level Performance Evaluation of the four protocols

- Table 5 shows summery of the comparative metric results for the four protocols for N =4 and n = 4

Table 5. Implementation results for the Binary, Query, Improved-Query, and Combined-Binary-Query protocols for N = 4 and n = 4

Metrics	Binary	Query	Improved-Query	Combined
Clock cycles (Clk)	31	42	41	27
Total capacitance (pF)	0.99641	1.156905	1.317833	1.49723
Switching power (uW)	4.1094	4.4749	5.1409	5.9422
Internal power (uW)	31.593	31.838	33.044	32.653
Leakage power (uW)	0.028176	0.027653	0.031744	0.029359
Total power (uW)	35.731	36.341	38.217	38.625
Total activity	574	746	873	757
Total Energy (pJ)	55.38305	76.316	78.345	52.144
Physical parameters				
# of cells	23	23	25	34
# of nets	28	28	31	39
# of pins	85	90	99	123
# of I/Os	5	5	5	5

- With equal read-time (clock cycles): Total power for Combined = 33.64 uW as compared to that of binary of 35.731uW.

Layout-level Performance Evaluation of the four protocols

- From Table 5, we see that
  - total clock cycles obtained from simulation results exactly matches the predicted clock cycles from protocol level analysis
  - Other metrics, such as power and energy do not reflect the results obtained in protocol level analysis, because
    - power analysis in protocol level was confined to state transitions only, but in layout level it was highly dependant on total capacitance and total switching activity.
  - The Combined Binary-Tree protocol is better than the rest of the three tree protocols in terms of all the used metrics.

Conclusion

- Protocol-level performance analysis for anti-collision protocols in RFID systems was studied
- Since the performance of a particular protocol depends on the ID distribution of the tags, discussions are confined to the worst-case scenario for a given number of tags available
- In particular, an improved protocol that combines the binary-tree and query-tree protocols was proposed.
- In protocol level, for binary-tree, query-tree, improved-query tree and combined query-tree, formulas for the number of state transitions and clock cycles were derived
- Simulation, synthesis and implementation for all protocols were done
- It has been shown that the new protocol has better performance in terms of speed, power and energy dissipation.

References

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