High Level Device Design: A Digital Camera

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Seminar Overview

Purpose

Design a low cost, high-speed, digital camera with a USB 2.0 interface.

Overview

- Design Objectives
- Camera Design Flow
- Component Selection
- Reconfigurable Hardware
- PCB Layout
- Future Development
- Conclusion

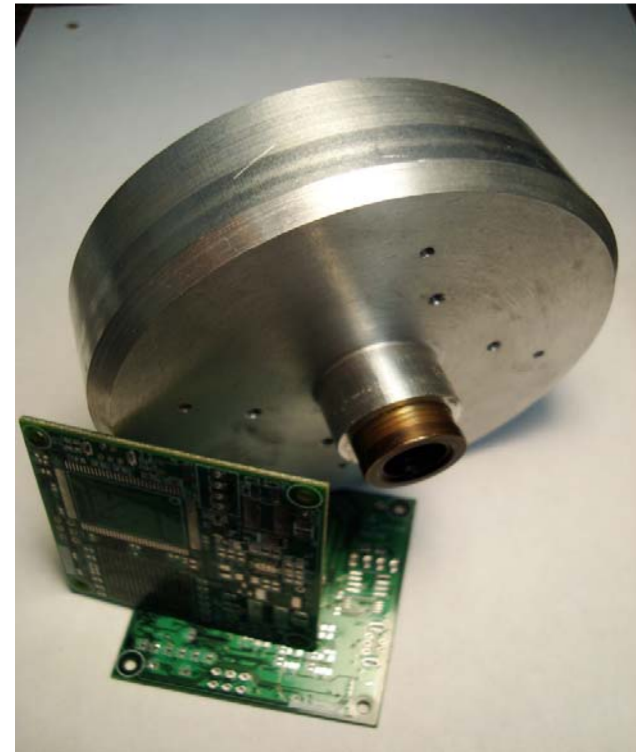


Fig 1. Camera PCB and Enclosure

Design Objectives

General Specifications

Communication Interface

- USB 2.0 Data communication.
- 3.3V I/O triggers.
- I2C external device communication.

Imaging

- 3 mega pixel colour images.
- 6 frames per second minimum transfer.

Processing

- Reconfigurable embedded system (upgradeability).

Memory

- EEPROM for device settings.

Camera Design Flow

Bottom-Up Methodology

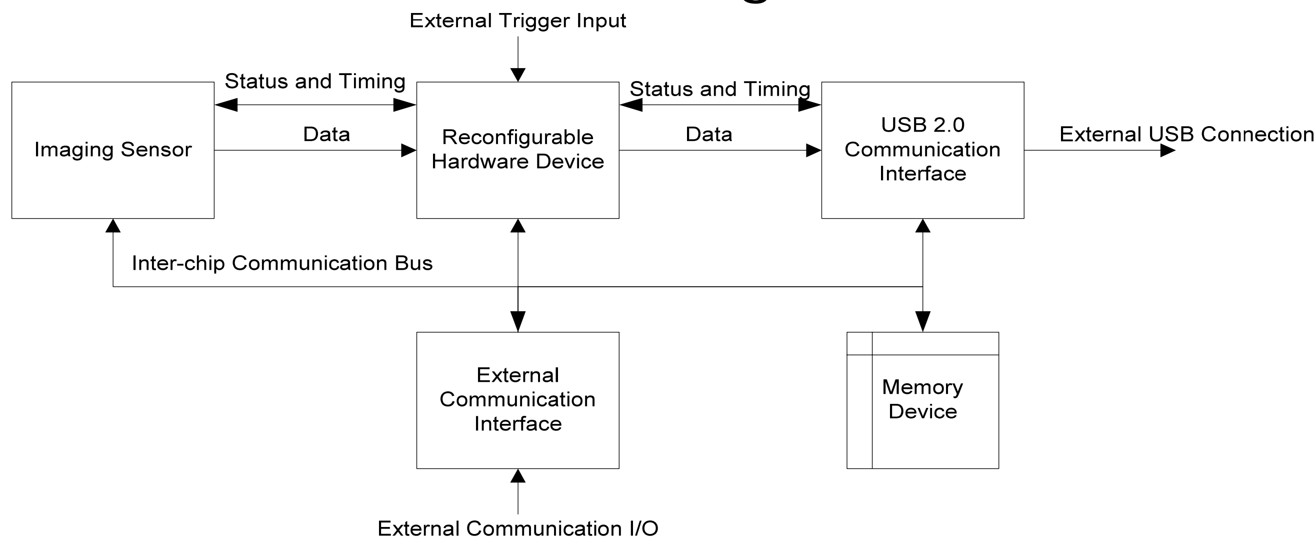
1) Select specific components.
2) Program desired component operation.
3) Combine components to prototype device.
4) Combine component groups on single PCB
5) “Tweak” as necessary.

Design Specifications
Hardware Selection
Hardware Coding
Test Bench Success?
No
Yes
Hardware Prototyping
Successful Implementation ?
No
Device Prototyping
Desired Device Operation?
No
Yes
PCB Layout and Device Placement
Troubleshooting
Successful Implementation ?
No
Yes
Firmware Revisons
Successful Implementation ?
No
Yes
System Integration

Component Selection

Required Hardware

1) Imaging sensor.
2) USB 2.0 microcontroller.
3) Reconfigurable device (FPGA or CLPD).
4) External system communication (ie. I2C bus).
5) Small EEPROM for device settings.



Component Selection

Imaging Sensor (CCD or CMOS?)

- From our design specifications:
  - Inspect flaws 0.1mm in size -> 1024x768 resolution
  - Colour
  - Satisfy required throughput (250 caps/min) -> 6 fps
  - Low Cost -> Supporting hardware and development.

Performance	CCD	CMOS
Responsivity	Moderate	Slightly better
Dynamic Range	High	Moderate
Uniformity	High	Low to Moderate
Uniform Shuttering	Fast, common	Poor
Speed	**Moderate to High**	**Higher**
Windowing	**Limited**	**Extensive**
Antiblooming	High to none	High
Biasing and Clocking	**Multiple, higher voltage**	**Single, low-voltage**

Component Selection

FPGA Selection

- From our design specifications:
  - Memory size -> Image line buffering and FIFO buffer.
  - Logic capacity -> Sophisticated image reconstruction.
  - Development Time -> Minimize.
  - Footprint -> Small to meet PCB area constraints.
  - I/O capacity -> Insignificant.

Series	Domain	Description	Cost (CAD)
Spartan-3A DSP	DSP – Optimized	For applications where integrated DSP MACs and expanded memory are required.	$140 to $215
Spartan-3AN	Non-Volatile	For applications where non-volatile, system integration, security, large user flash are required.	$13 to $80
Spartan-3A	I/O Optimized	Ideal for bridging, differential signalling and memory interfacing applications, requiring wide or multiple interfaces and modest processing.	$63 to $88
Spartan-3E	**Logic Optimized**	**Ideal for logic integration, DSP co-processing and embedded control, requiring significant processing and narrow or few interfaces.**	**$11 to $75**
Spartan-3	I/O + Logic Optimized	Ideal for highly-integrated data-processing applications.	$10 to $130

Component Selection

External/ Internal Communication Bus

- USB 2.0 device communication.
  - Via widely used available Cypress USB microcontroller.
  - Auto-commit USB data packets with 4 buffers for uninterrupted data transfer.
  - Data rates up to 40MBps.
  - Very small MINI-B connectors.

- Inter-Integrated Circuit (I^2C) bus.
  - I2C bus extender for external communication.
  - Widely supported on most IC devices.
  - Interface with EEPROM for device settings.

- 3.3V I/O for triggers and debugging.

Component Selection

Power Supplies

- 3.3V, 2.5V and 1.2V for FPGA power.
- 3.3V digital for Cypress chip and supporting ICs.
- 3.3V digital for Micron imaging sensor.
- 3.3V analog for Micron imaging sensor.

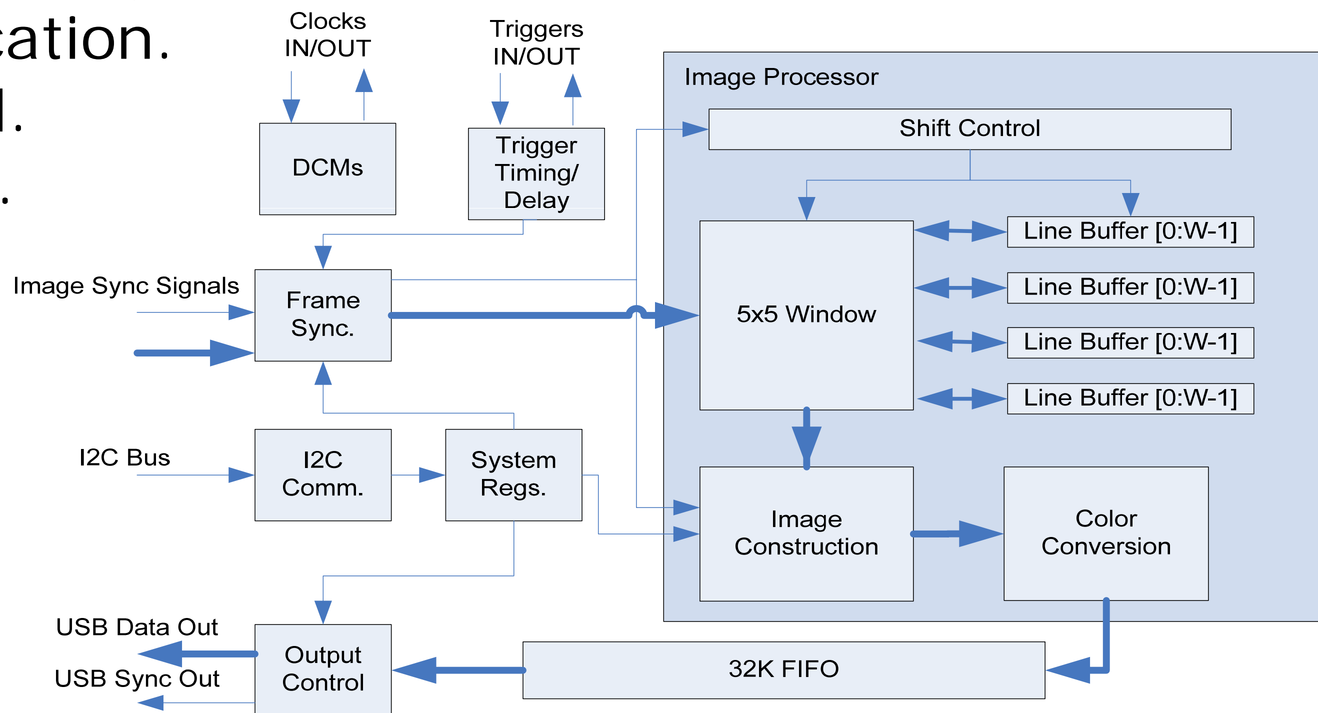
TPS75003 Triple Supply

- Non-synchronous buck converters (up to 3A for I/O and core.)
- Low Dropout linear regulator (300mA for aux power)
- Soft start feature to prevent inrush current during start up and provide desired voltage ramps for FPGA power.

Reconfigurable Hardware

FPGA Overview

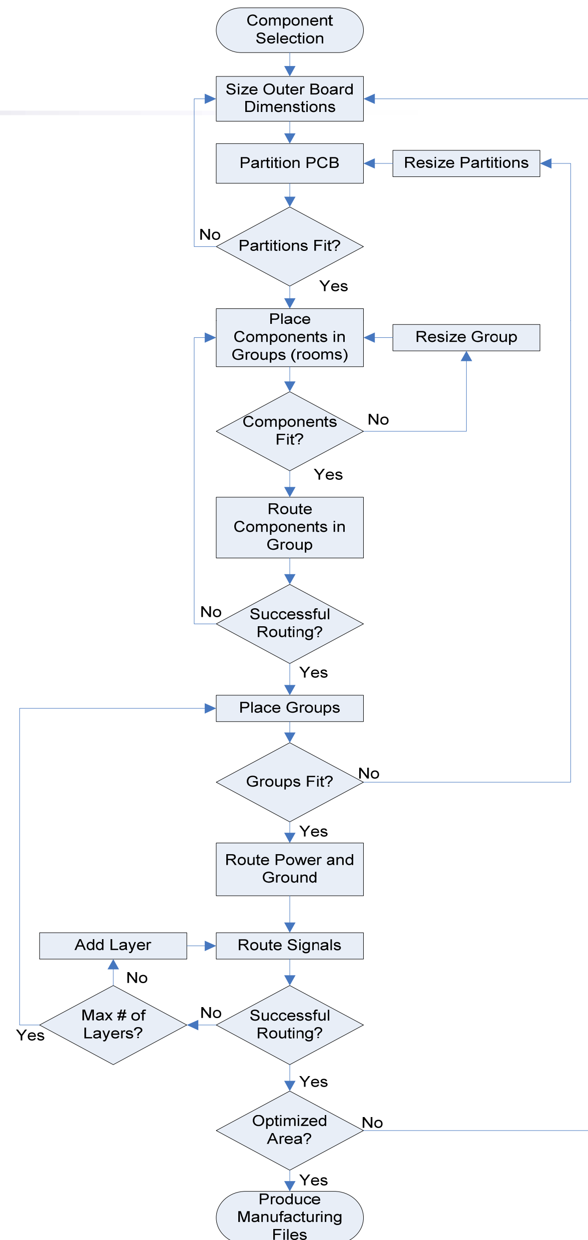
- Frame timing and data synchronization.
- Image processing (demosaicking and enhancement.)
- Digital Clock Management (DCM).
- I2C Communication.
- Output Control.
- Data buffering.
- Trigger Delay.



PCB Design

PCB Design Considerations

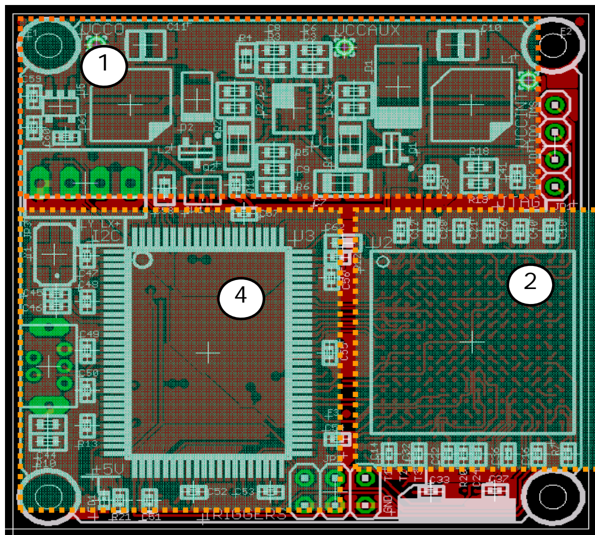
- PCB dimensions and layers.
- Component Placement.
- Power and Ground planes and routing.
- Bypass capacitor sizing and placement.
- Vias
- Data bus routing.
- Trace widths and signal routing.
- I/O connector placement and clearance.
- Silk screening

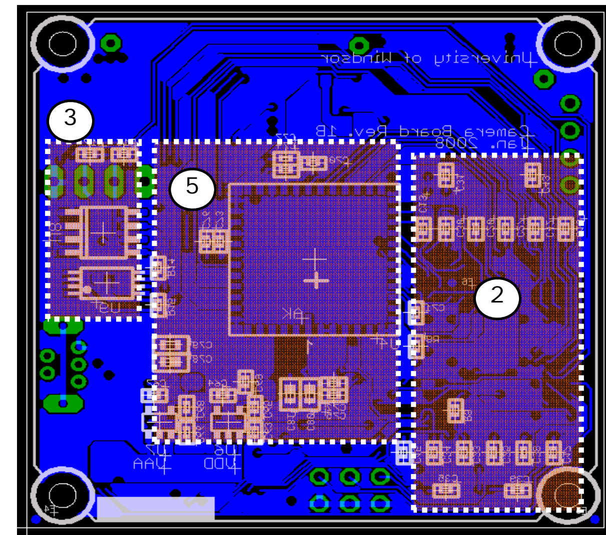


PCB Design

PCB Component Groups

1) Power Supply
2) FPGA
3) I2C Components
4) Cypress USB MCU
5) Micron Imaging Sensor

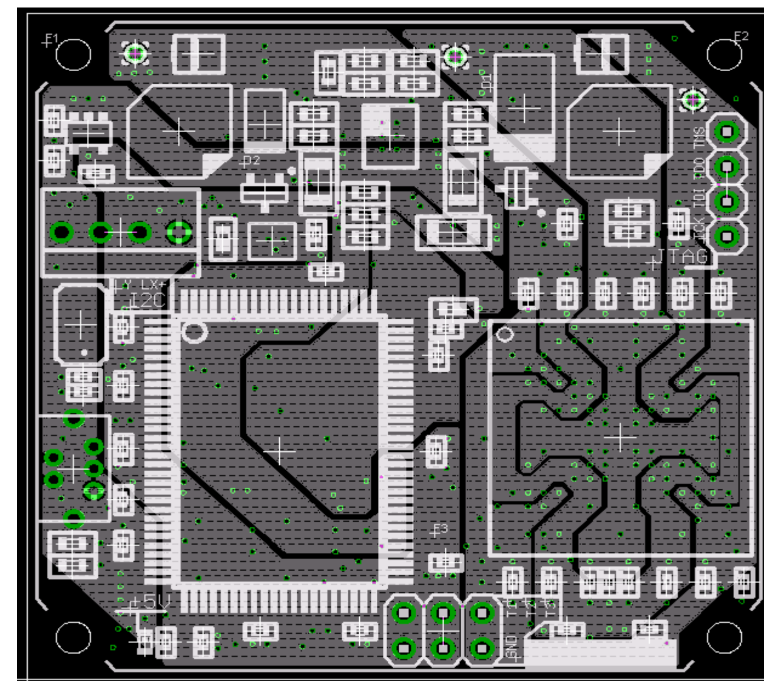




PCB Design

Power and Ground Planes

- Maximize area of power planes.
  - Greater capacitance to parallel ground plane.
- Minimize bends and loops.
  - Reduce “Spreading Inductances”.
- Ideally, separate plane for every source.
  - Noisy planes nearest to surface layers to minimize via lengths.



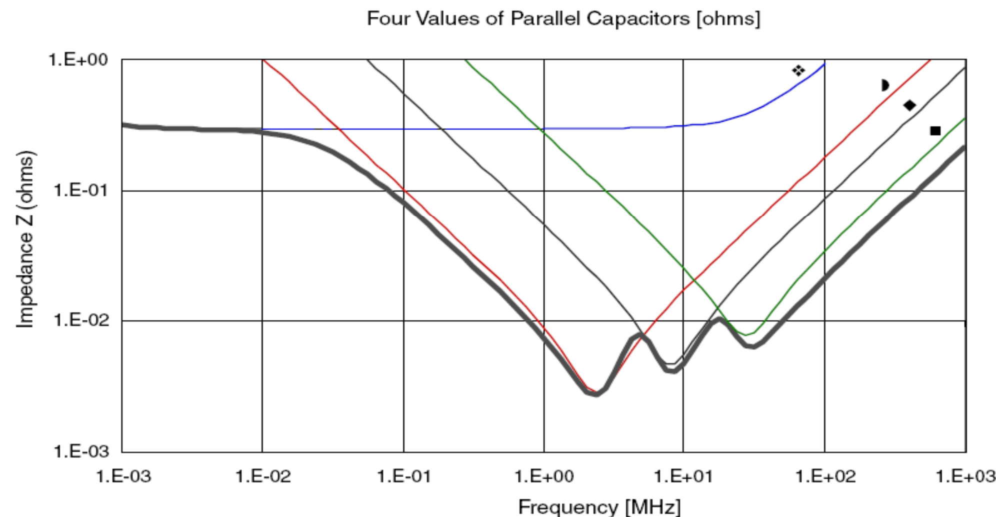
- Separate analog and digital ground planes.
- Copper fill free surface space with ground plane.

PCB Design

Decoupling Capacitance

- Create a low, flat, power supply impedance over the operating frequency range: typ. 500kHz-500MHz
- Place one capacitor per power pin.
- Utilize a range of cap values.
  - Small caps have less impact on total impedance profile and hence more are required.
- Example 48pin design:

Quantity	Symbol	Package	Capacitive Values (μF)	Parasitic Inductance (nH)	Parasitic Resistance (ohms)
2	❖	E	680	2.8	0.57
7	◗	0805	2.2	2.0	0.02
13	◆	0603	0.22	1.8	0.06
26	■	0402	0.022	1.5	0.20

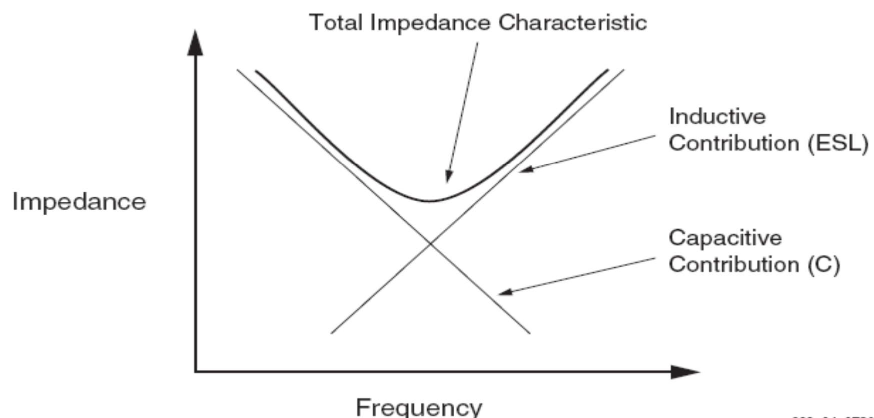


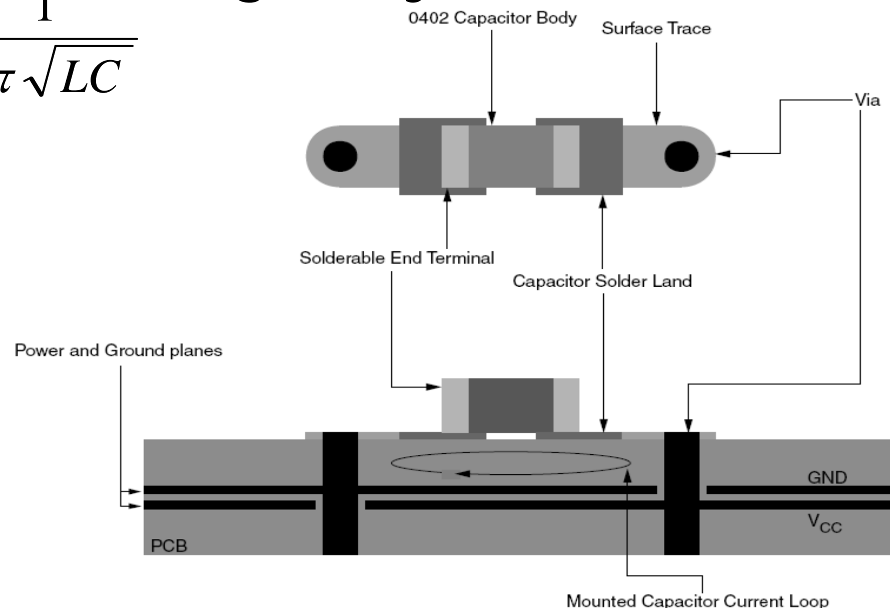
PCB Design

Decoupling Capacitance cont.

- Placement is critical!
  - Minimize trace and via lengths to reduce inductance.
  - Transmission delay of current introduces latency in the capacitors response to fluctuations in the PDS.
- Effective resonant frequency varies greatly from "self" resonant frequency.

$$F_R = \frac{1}{2\pi\sqrt{LC}}$$

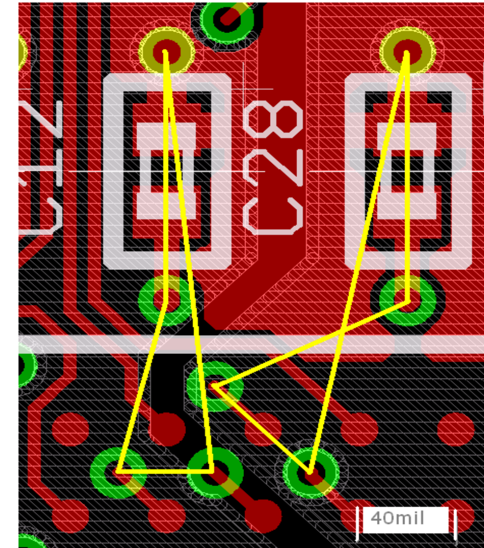


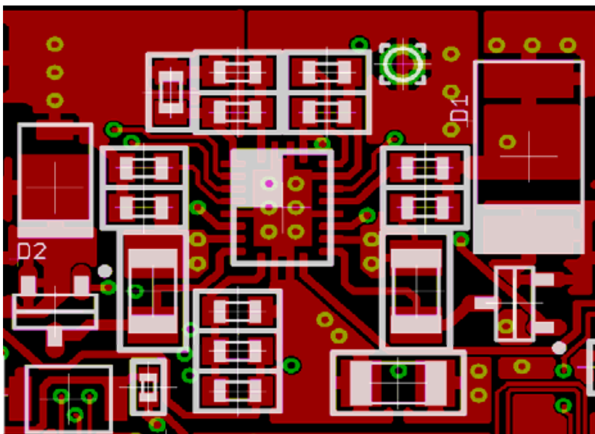


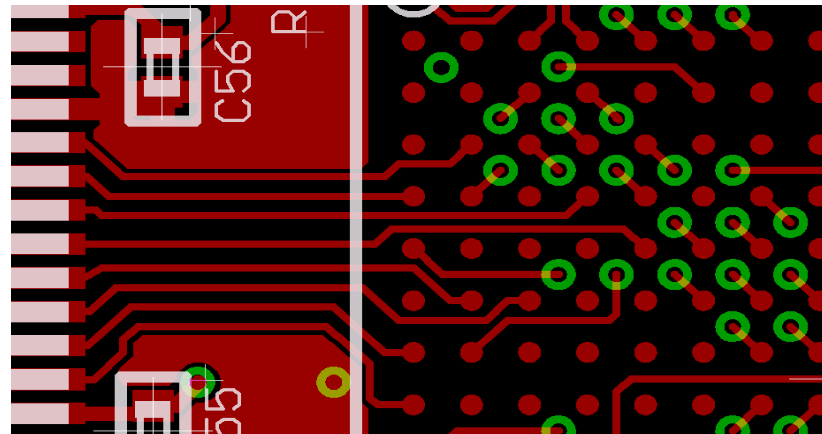
PCB Design

Component Placement

- Component spacing.
- Critical trace widths and spacing.
- Successful routing.
- Critical paths.
  - Signal Delay
  - Parasitic Inductance
- Copper fill.







PCB Design

Manufacturing Files

- PCB “stack-up” layer information.
- Copper etch.
- Solder mask.
- Solder paste.
- Silk screen.
- Drill holes.
- Board machining.
- Component placement.

Future Development

Image Processing

- Incorporate more sophisticated algorithms for image reconstruction.
- Alternate colour formats.
- Image compression.

Communication

- Enhanced error checking and reporting.
- Debugging output features.
- Improve I2C communication in reconfigurable device.

Future Development

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[2] H.S. Malvar, He Li-wei, R. Cutler, "High-quality linear interpolation for demosaicing of Bayer-patterned color images," IEEE International Conference on Acoustics, Speech, and Signal Processing, vol. 3, pp485-8, May 2004.

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[4] T. Komatsu, T. Saito, T., "Super-Resolution Sharpening-Demosaicking Method for Removing Image Blurs Caused by An Optical Low-Pass Filter," IEEE International Conference on Image Processing, vol. 1, pp. 845-8, Sept. 2005

[5] B. Shan, W. Wang, T. Shen, J. LV, "Research and Implementation of a Multiple Channel CMOS Image Sampling System," The 8th International Conference on Signal Processing, vol. 1, 2006

[6] "Four- and Six-Layer, High-Speed PCB Design for the Spartan-3E FT256 BGA Package", Xilinx Application Note: Spartan-3E Family, XAPP289, October 2006

[7] D. Litwiller, "CCD vs CMOS: Facts and Fiction," Photonics Spectra, Laurin Publishing Co. Inc., Jan. 2001

[8] ½-Inch 3-Megapixel Digital Image Sensor MT9T001DS. www.micron.com/imaging