4:2 COMPRESSOR DESIGN BASED ON DOMINO LOGIC

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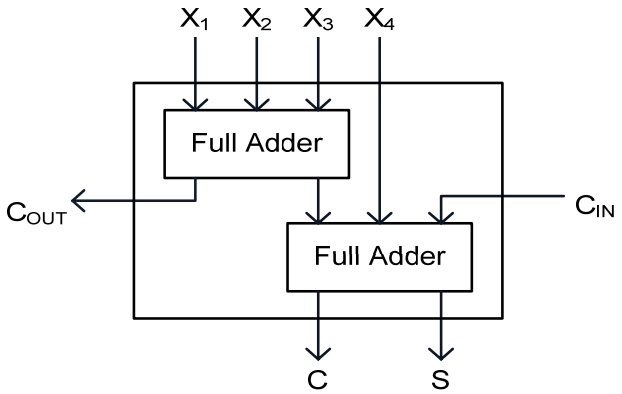
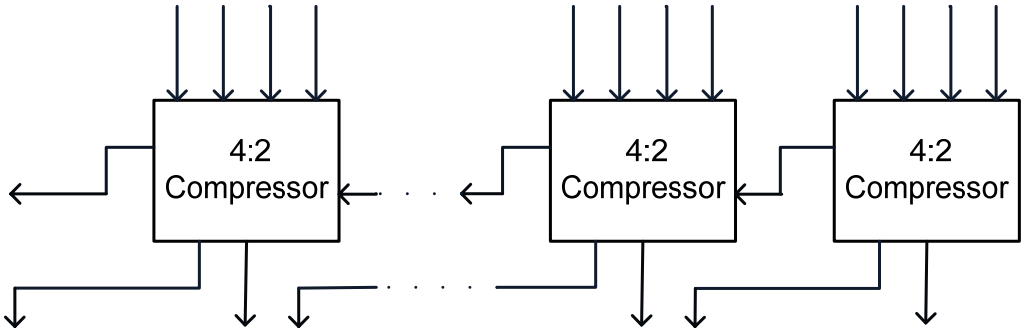
Outline

- 4:2 Compressors
- Domino logic
- Logical decompositions of 4:2 compressors
- Circuit level optimization – Split Domino Logic
- Simulation results and Conclusion

4:2 Compressors



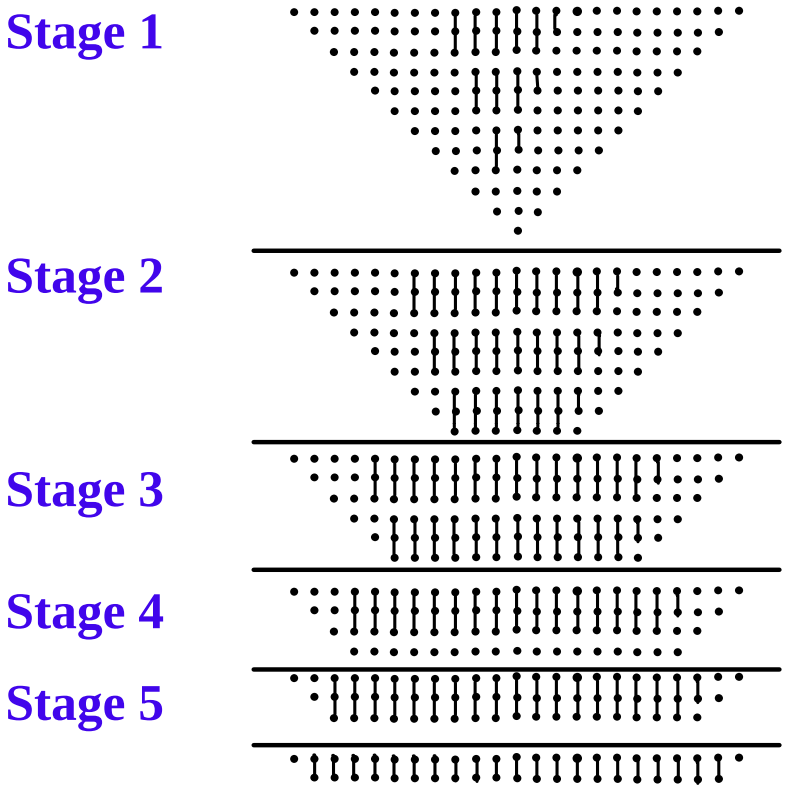
4:2 Compressor



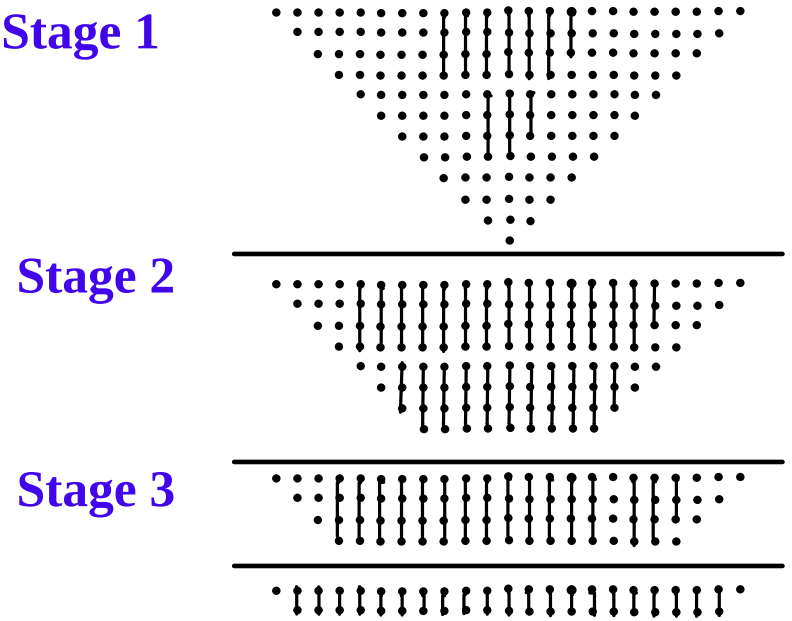
4:2 Compressor Array

- The 4:2 compressor takes five equally weighted inputs (C_{IN}, X_1, X_2, X_3, X_4) and generate a sum bit (S), a carry-bit (C) and a carry-propagate-bit (C_{OUT}).
- The 4:2 compressor array is formed by a series of 4:2 compressors cascaded together, it is used to perform column-wise compression of the partial product.

Analysis of 3:2 and 4:2 Reduction Scheme (12×12 Dadda Tree)



3:2 Reduction Scheme



4:2 Reduction Scheme

Analysis of 3:2 and 4:2 Reduction Scheme

Max column height per stage of a 3:2 scheme (carry save array)

h	0	1	2	3	4	5	6	7	8	9	10
n(h)	2	3	4	6	9	13	19	28	42	63	94

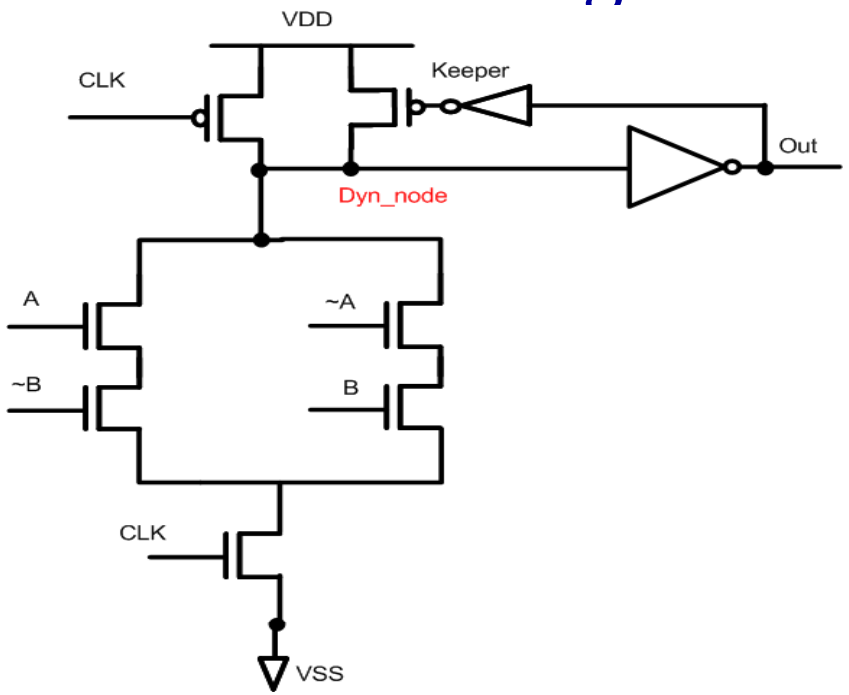
Max column height per stage of a 4:2 scheme (4:2 compressor)

h	0	1	2	3	4	5	6	7
n(h)	3	4	8	16	32	64	128	256

“ *n(h)* ” represents max column height

“ h ” represents the number of stages

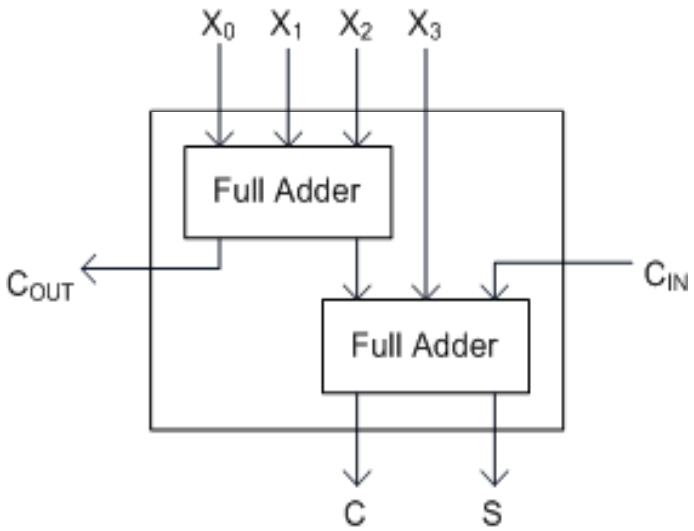
Domino Logic



An example of domino XOR gate

- It is consist of a pull-down network, clocked PMOS and NMOS transistors.
- Its operation is divided into two major phases: precharge (CLK=0) and evaluation (CLK=1).
- Advantages: lower transistor count, faster switching speed, no short circuit current.
- Disadvantages: charge leakage, charge sharing and etc.

Logical Level Decomposition of 4:2 Compressors



Configuration of 4:2 compressor

$$X_0 + X_1 + X_2 + X_3 + C_{IN} = Sum + 2 \cdot (Carry + Cout)$$

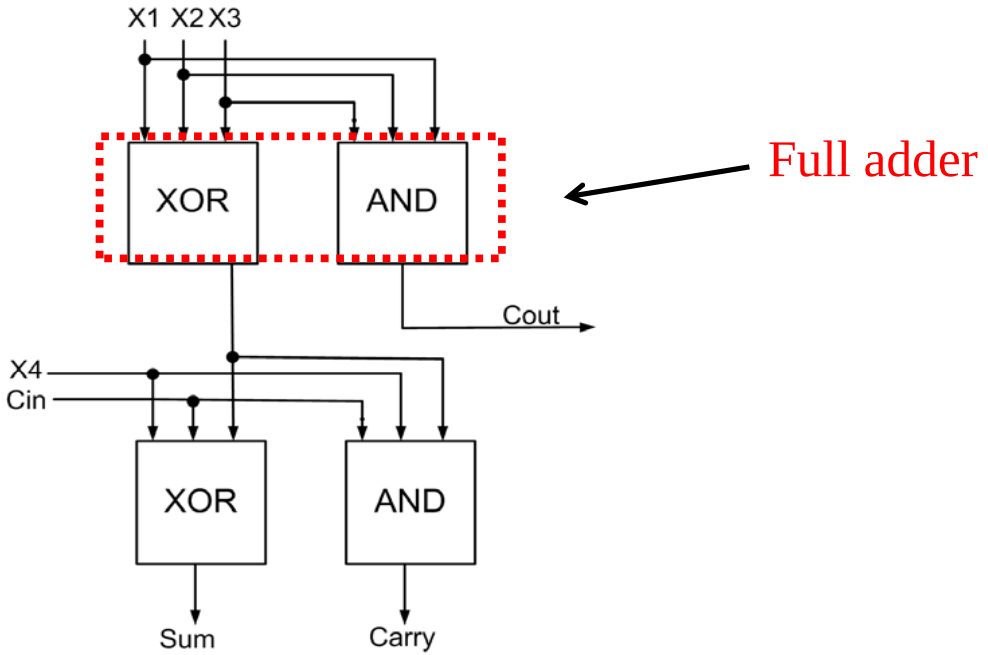
$$S = S \oplus X_4 \oplus C_{IN} = X_0 \oplus X_1 \oplus X_2 \oplus X_3 \oplus C_{IN}$$

$$\begin{aligned} C &= (S \oplus X_3) \cdot C_{IN} + S \cdot X_3 \\ &= (X_0 \oplus X_1 \oplus X_2 \oplus X_3) \cdot C_{IN} \\ &+ \overline{(X_0 \oplus X_1 \oplus X_2 \oplus X_3)} \cdot X_3 \end{aligned}$$

$$C_{out} = (X_0 \oplus X_1) \cdot X_2 + X_0 \cdot X_1 = (X_0 \oplus X_1) \cdot X_2 + \overline{(X_0 \oplus X_1)} \cdot X_0$$

4:2 compressor could be realized by different combinations of XOR Gates, AND Gates and MUXs.

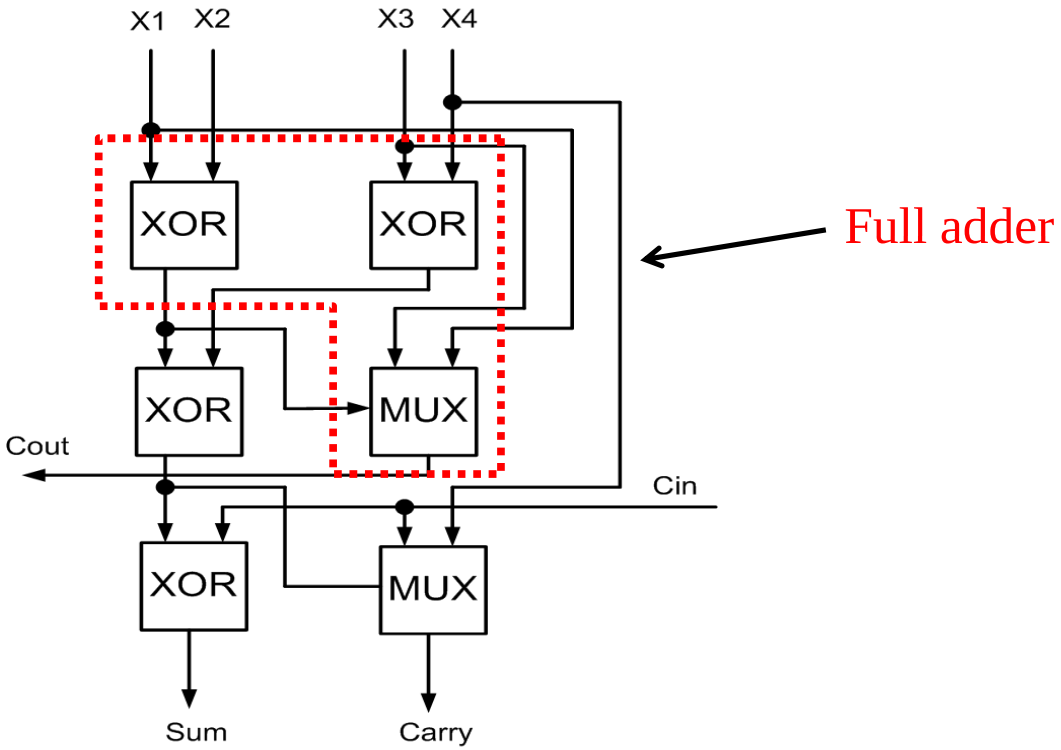
Logical Level Decomposition of 4:2 Compressors



Primitive decomposition of 4:2 compressor (Com_and)

- It is formed by using 3-input XOR gates and 3-input AND gates.
- Its regularity lends itself to gains at the architecture level of the multiplier.
- The critical path of the compressor is 4 XOR gates.

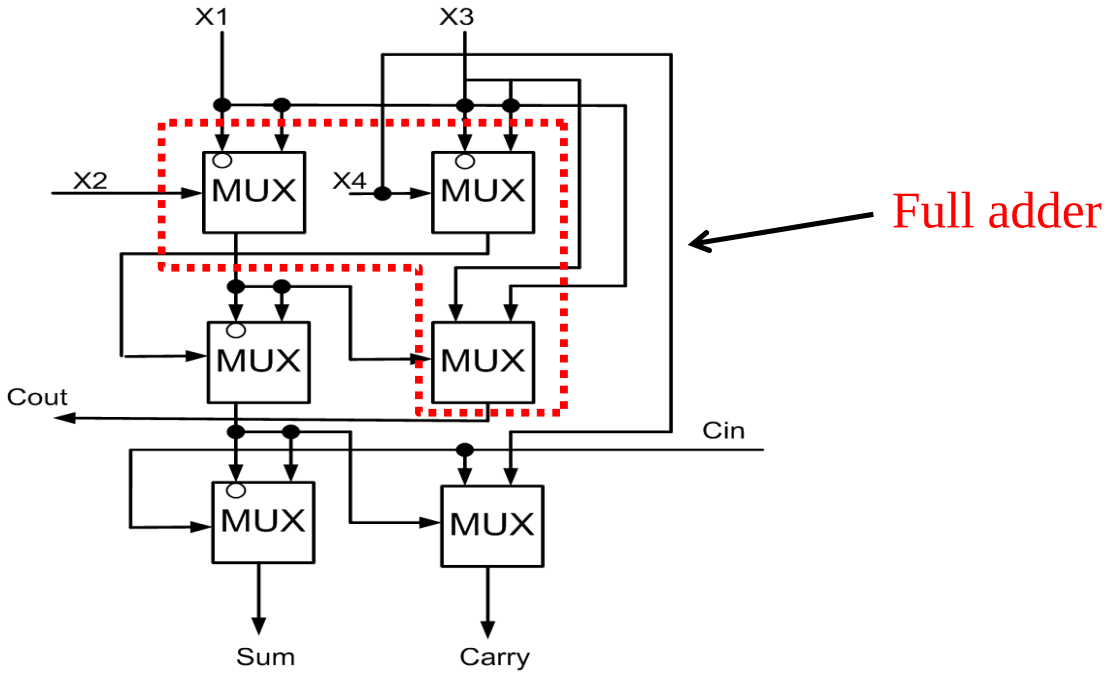
Logical Level Decomposition of 4:2 compressors



Alternative decomposition of 4:2 compressor (Com_mux)

- It is composed of six modules: four 2-input XOR gates and two 2:1 MUX gates.
- 2:1 MUX gate is used instead of AND gate to generate two carry signals “Carry” and “Cout”.
- The critical path of the compressor is 3 XOR gates.

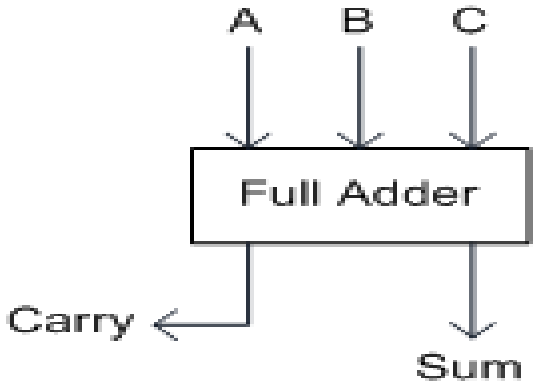
Logical Level Decomposition of 4:2 Compressors



Alternative decomposition of 4:2 compressor (Com_pur_mux)

- It consist of six 2:1 MUX gates.
- All three outputs: “Sum”, “Carry” and “Cout” are generated by using 2:1 MUX gates.
- The critical path delay of the compressor is 3 XOR gates.

Optimization of 4:2 Compressors



Configuration of full adder

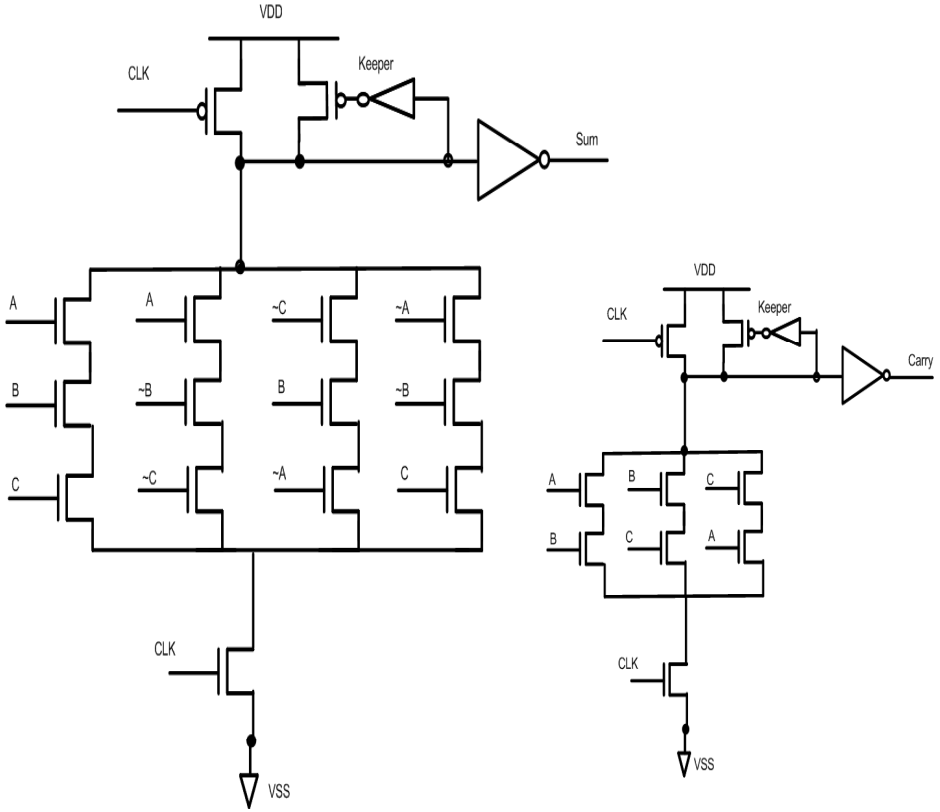
$$Sum = A \oplus B \oplus C = ABC + \overline{A}\overline{B}C + A\overline{B}\overline{C} + \overline{A}B\overline{C}$$

$$Carry = AB + BC + AC$$

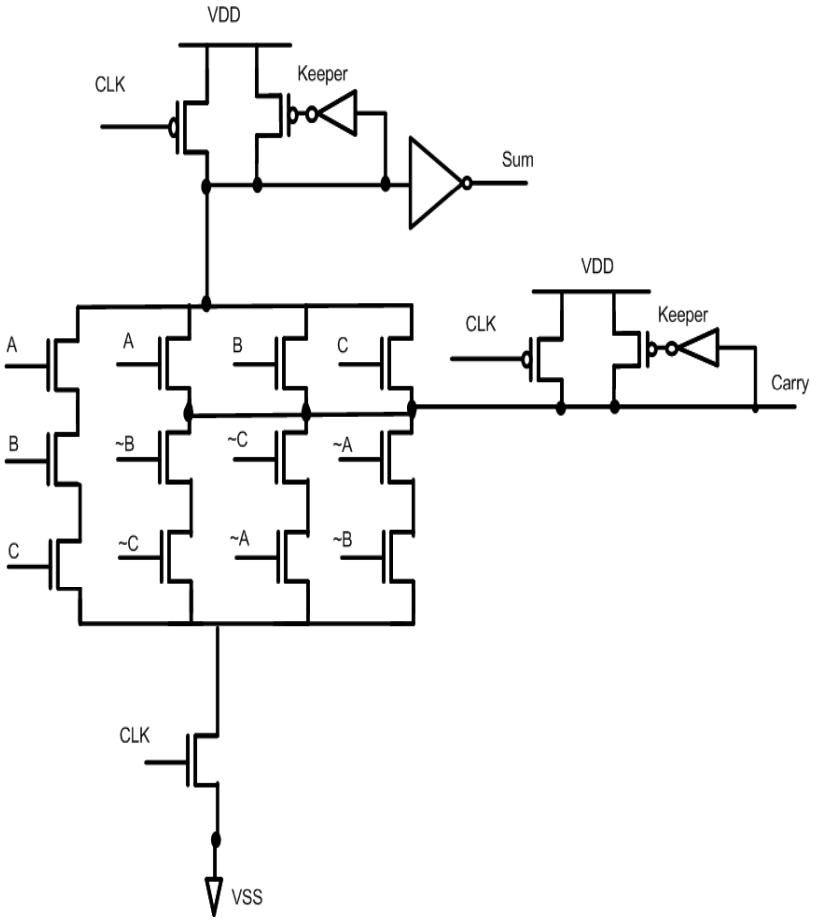
$$\overline{Carry} = \overline{A}\overline{B} + \overline{B}\overline{C} + \overline{A}\overline{C}$$

By taking the NOT of Carry, we could use part of the circuit, which generates Sum signal, to generate Carry signal. Thus the lower transistor count and higher performance of full adder could be achieved.

Optimization of 4:2 Compressors

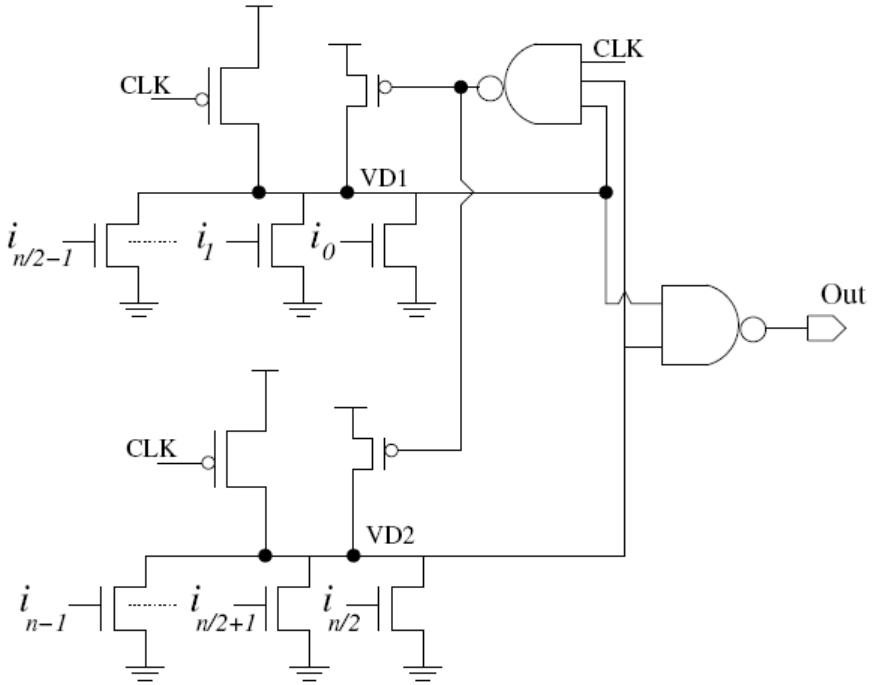


Conventional full adder using Domino Logic



Proposed full adder using Domino Logic

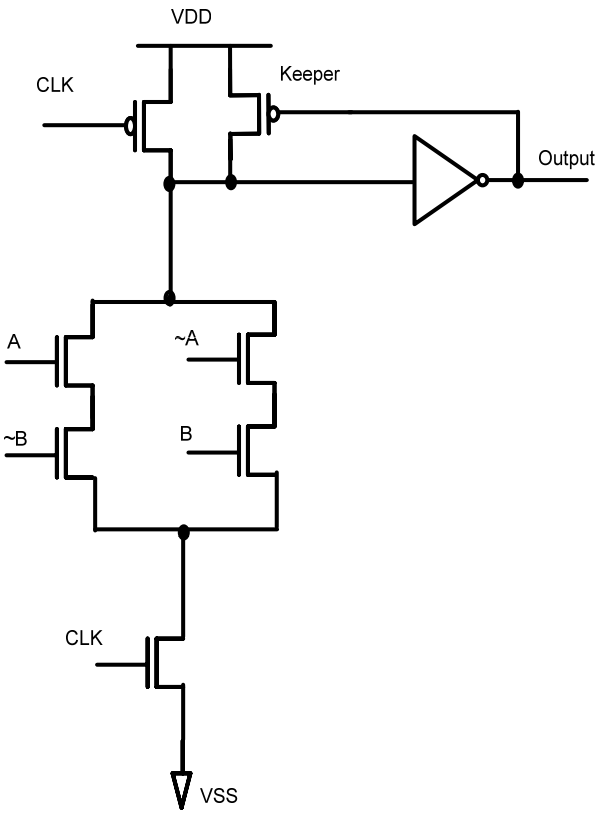
Split Domino Logic

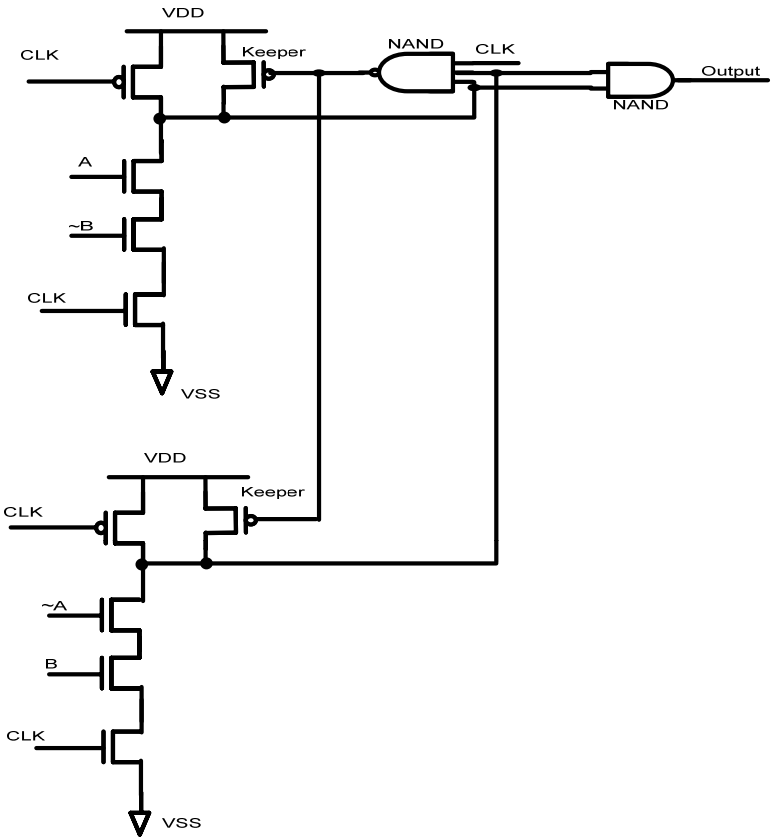


N-input Split Domino OR gate

- The pull down network is equally divided into two sub-network, a logical 2-input NAND gate is used to generate the output. The large keeper transistor is also replaced by two smaller transistors.
- The main advantage of Split Domino is to reduce the dynamic node capacitance and consequently fast evaluation.

Split Domino Logic – XOR Gate

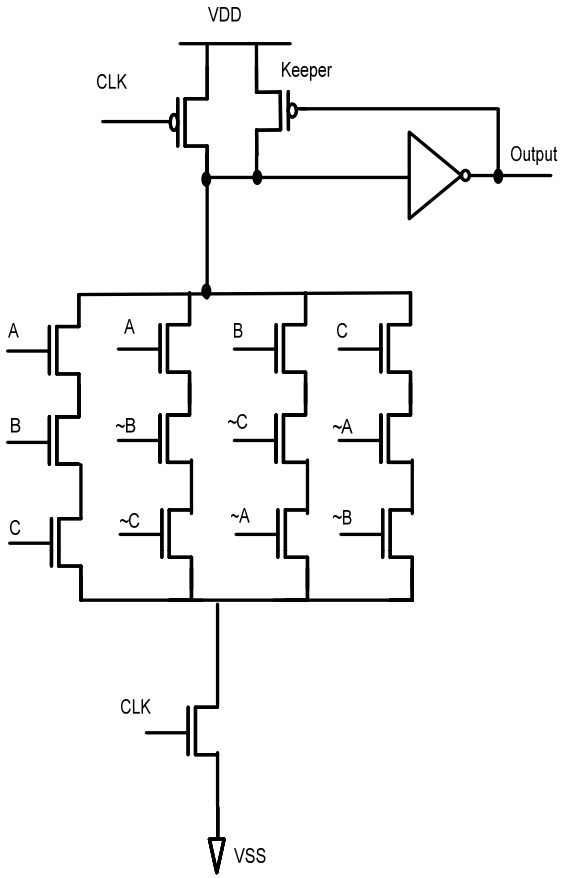




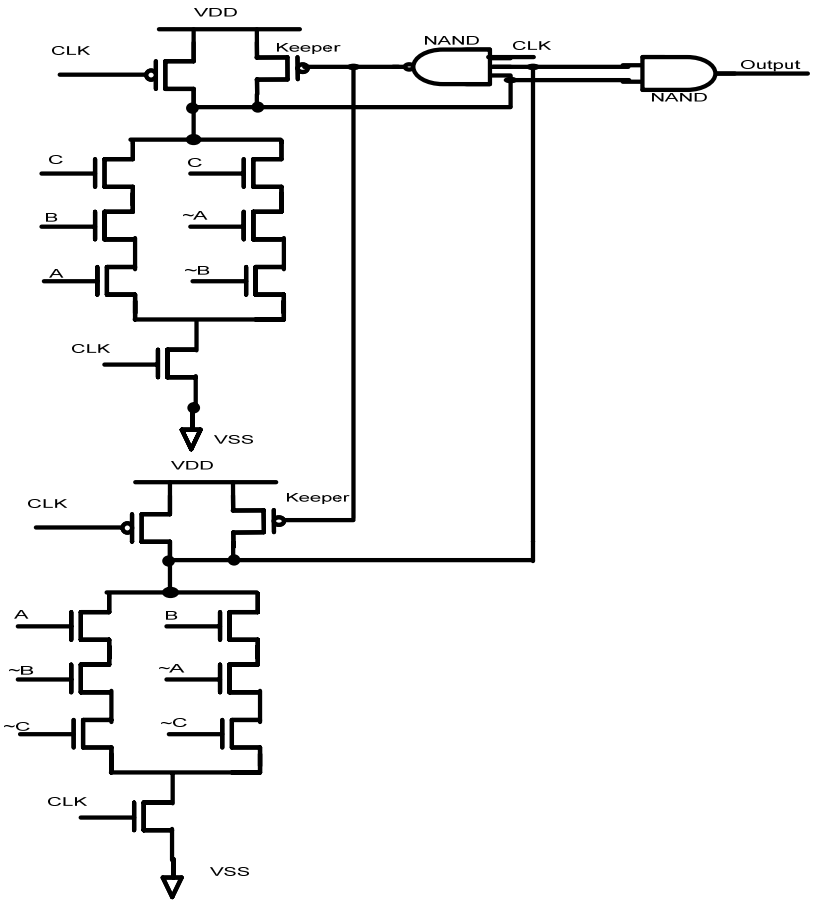
2-input XOR Gate using Domino Logic (denoted as "2_xor_D")

2-input XOR Gate using Split Domino Logic (denoted as "2_xor_SD")

Split Domino Logic – XOR Gate

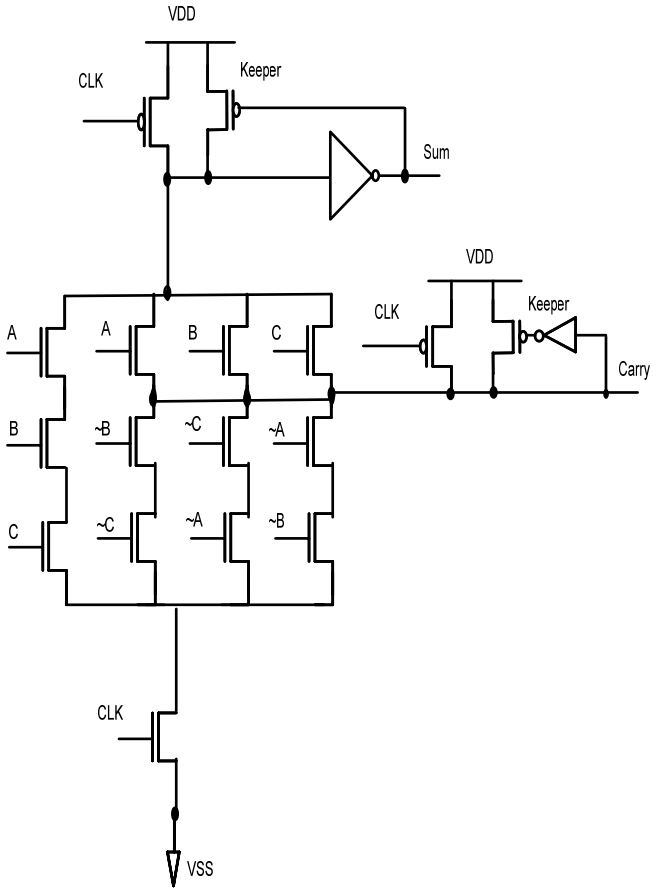


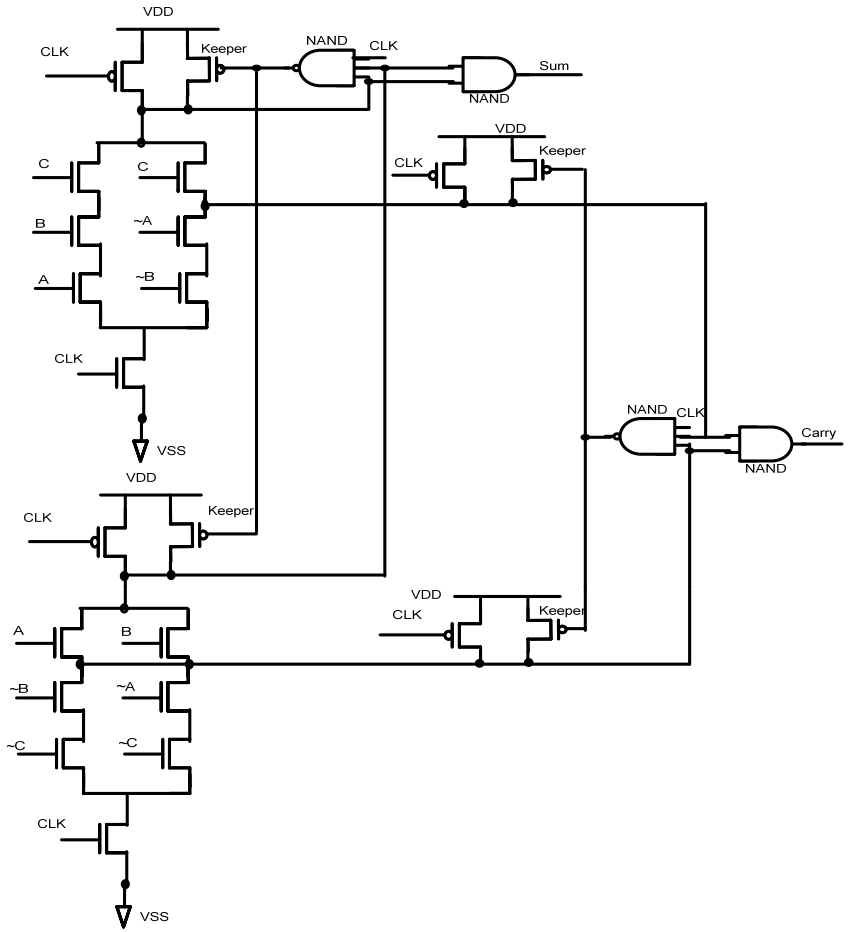
3-input XOR Gate using Domino Logic (denoted as "3_xor_D")



3-input XOR Gate using Split Domino Logic (denoted as "3_xor_SD")

Split Domino Logic – Full Adder





Proposed full adder using Domino Logic (denoted as “FA_new”)

Proposed full adder using Split Domino Logic (denoted as “FA_SD”)

Simulation Result

- 2-input XOR Gate, 3-input XOR Gate, Full adder and 4:2 Compressors are designed in Domino Logic and Split Domino Logic style separately. The simulations are performed by using HSPICE in Cadence design tool. All the circuits are targeted for TSMC 0.18 technologies.

- In the test bench, each input is driven by buffered signals and each output is loaded with buffers, which offer a realistic simulation environment reflecting the operation in actual applications.

- The delay is measured from the time at which the input signals reaching 50% of its full value to the time when the output signal reaching 50% of its full potential. The average delay is the average of delays of all input data. The worst case delay is the largest delay among all input data.

- Circuits are thoroughly tested by all the possible input vector combinations at 1.8 voltage source.

Simulation Result

Simulation Results for logical decompositions of 4:2 Compressors

Cell Name	Power Dissipation (ns)	Average Delay (ns)	Worst Case Delay (ns)	Average PDP	Worst Case PDP	Operation Frequency (GHz)
Com_and	2.48E-04	0.47	0.59	1.17E-13	1.46E-13	1
Com_mux	3.12E-04	0.57	0.89	1.78E-13	2.78E-13	0.41
Com_pur_mux	2.81E-04	0.51	0.80	1.43E-13	2.25E-13	0.63

Comparison of different logical decompositions of 4:2 Compressors

Cell Name	Power Dissipation (ns)	Average Delay (ns)	Worst Case Delay (ns)	Average PDP	Worst Case PDP	Operation Frequency (GHz)
Com_and	100%	100%	100%	100%	100%	100%
Com_mux	126%	121%	151%	154%	190%	41%
Com_pur_mux	113%	109%	136%	122%	154%	63%

Simulation Result

Simulation Results for 2-input XOR Gates

Cell Name	Power Dissipation (w)	Average Delay (ns)	Worst Case Delay(ns)	Average PDP	Worst Case PDP	Operation Frequency (GHz)
2_xor_D	1.01E-04	0.17	0.24	1.72E-14	2.42E-14	2.63GHz
2_xor_SD	2.26E-04	0.22	0.39	4.97E-14	8.81E-14	2.17GHz
% Savings	224%	129%	165%	288%	364%	82.5%

Simulation Results for 3-input XOR Gates

Cell Name	Power Dissipation (w)	Average Delay (ns)	Worst Case Delay (ns)	Average PDP	Worst Case PDP	Operation Frequency (GHz)
3_xor_D	1.06E-04	0.21	0.24	2.23E-14	2.54E-14	2.17
3_xor_SD	1.19E-04	0.15	0.28	1.79E-14	3.33E-14	2.38
% Savings	112%	71.4%	116%	80.3%	131%	109%

Simulation Result

Simulation Results for Full Adders

Cell Name	Power Dissipation (ns)	Average Delay (ns)	Worst Case Delay (ns)	Average PDP	Worst Case PDP	Operation Frequency (GHz)
FA_con	1.78E-04	0.28	0.41	4.98E-14	7.29E-14	1.92
FA_new	1.20E-04	0.29	0.51	3.48E-14	6.12E-14	1.67
FA_SD	1.32E-04	0.22	0.39	2.90E-14	5.15E-14	2.17

Comparison of different Full Adders

Cell Name	Power Dissipation	Average Delay	Worst Case Delay	Average PDP	Worst Case PDP	Operation Frequency
FA_con	100%	100%	100%	100%	100%	100%
FA_new	67%	104%	124%	70%	84%	87%
FA_SD	74%	79%	95%	58%	71%	113%

Simulation Result

Simulation Results for 4:2 Compressors

Cell Name	Power Dissipation	Average Delay	Worst Case Delay	Average PDP	Worst Case PDP	Operation Frequency (GHz)
Com_con	2.48E-04	0.47	0.60	1.17E-13	1.49E-13	1
Com_new	2.29E-04	0.42	0.53	0.96E-13	1.21E-13	1.25
Com_SD	2.27E-04	0.32	0.48	0.73E-13	1.09E-13	1.67

Comparison of different 4:2 Compressors

Cell Name	Power Dissipation	Average Delay	Worst Case Delay	Average PDP	Worst Case PDP	Operation Frequency
Com_con	100%	100%	100%	100%	100%	100%
Com_new	92%	89%	88%	82%	81%	125%
Com_SD	91%	68%	80%	62%	73%	167%

Conclusion

- Three different logical level decompositions of 4:2 compressor are implemented in Domino Logic, followed by the simulation results of these circuits.

- A new architecture of full adder is proposed, and used to implement 4:2 compressor in Domino Logic. Its property is confirmed by the simulation results.

- 2-input XOR Gate, 3-input XOR Gate, Full adder and 4:2 Compressors are implemented in Domino Logic and Split Domino Logic separately, simulation results confirm that Split Domino Logic outperform Domino Logic in terms of delay, power and operating speed.

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Thank You