Performance Analysis and Improvement for Hybrid CMOS-SET Circuit Architectures

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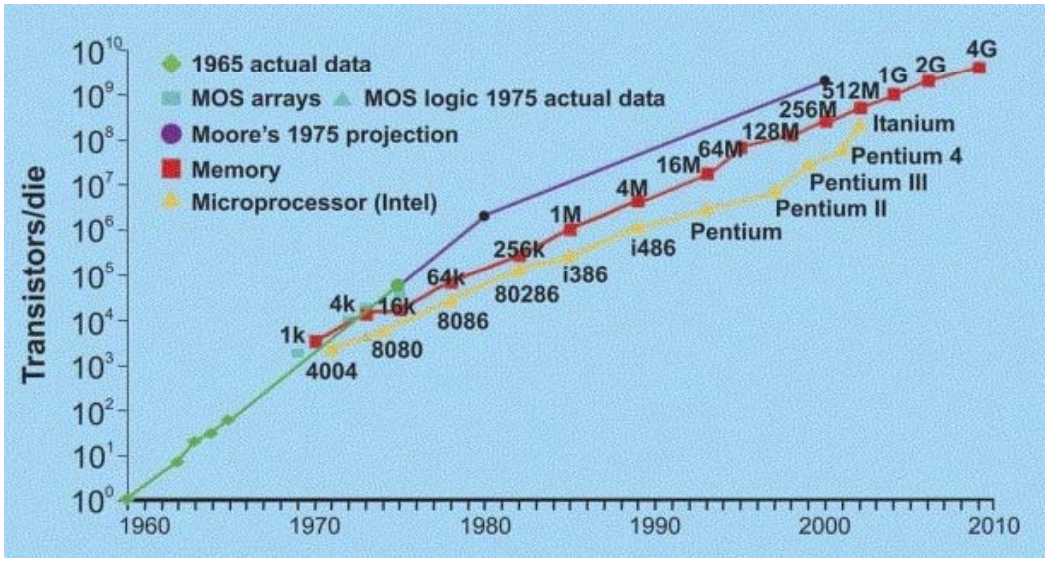
Overview

- Research Background - Why nanotechnology.
- Structure of SET transistor and Coulomb Blockade Oscillation.
- Why hybrid CMOS-SET circuits – Comparison between CMOS and SET.
- Simulation methodology of hybrid CMOS-SET circuits.
- Two of the most popular hybrid CMOS-SET architectures – serial SETMOS and parallel SETMOS.
- Analysis and compare of serial and parallel SETMOS in terms of power dissipation, drivability, and temperature effect.
- Voltage-biased parallel SETMOS with improved temperature effect.
- Implementation examples using parallel SETMOS architecture – Hybrid CMOS-SET NOR gate.

Research Background Introduction

- **Moore's Law**

  The number of transistors on a chip will double about every two years.



The scale-down of the size of MOSFET transistors according to Moore's law has taken place for the last 40 years, so far it has entered the deep sub-50 nm regime.

The more transistors on a chip, the higher performance and the lower cost of circuits are.

Research Background Introduction

- **CMOS scale-down limits**
  - **Physical limit**

    Quantum effects and non-deterministic behavior.

    - Never overcome
  - **Technical limit**

    Power dissipation, process variation, second-order effects, and design complexity.

    - Can be overcome, but difficult
  - **Economic limit**

    Update of facilities and techniques.

    - Can be overcome, but expensive

Research Background Introduction

- **Nanoelectronics – next generation technology.**

  Definition of nanoelectronics:

  Digital and signal-processing electronics, information storage devices, and electronic sensors that achieve enhanced performance by reducing feature sizes below 100 nm.

  In the field of nanoelectronics, people are able to control the movement and position of a small number of electrons instead of current with thousands of electrons.

Research Background Introduction

- **Emerging Nano-Devices: Life after CMOS**
  - ✓ **Single electron transistor (SETs)**
  - ✓ **Nanotube (CNTs)**
  - ✓ **Nanowires**
  - ✓ **Resonant tunneling diode (RTD)**
  - ✓ **Rapid single quantum flux (RSQF)**
  - ✓ **Nanoelectromechanical systems (NEMS)**
  - ✓ **Molecular devices**

Research Background Introduction

- **Single electron transistor (SETs)**

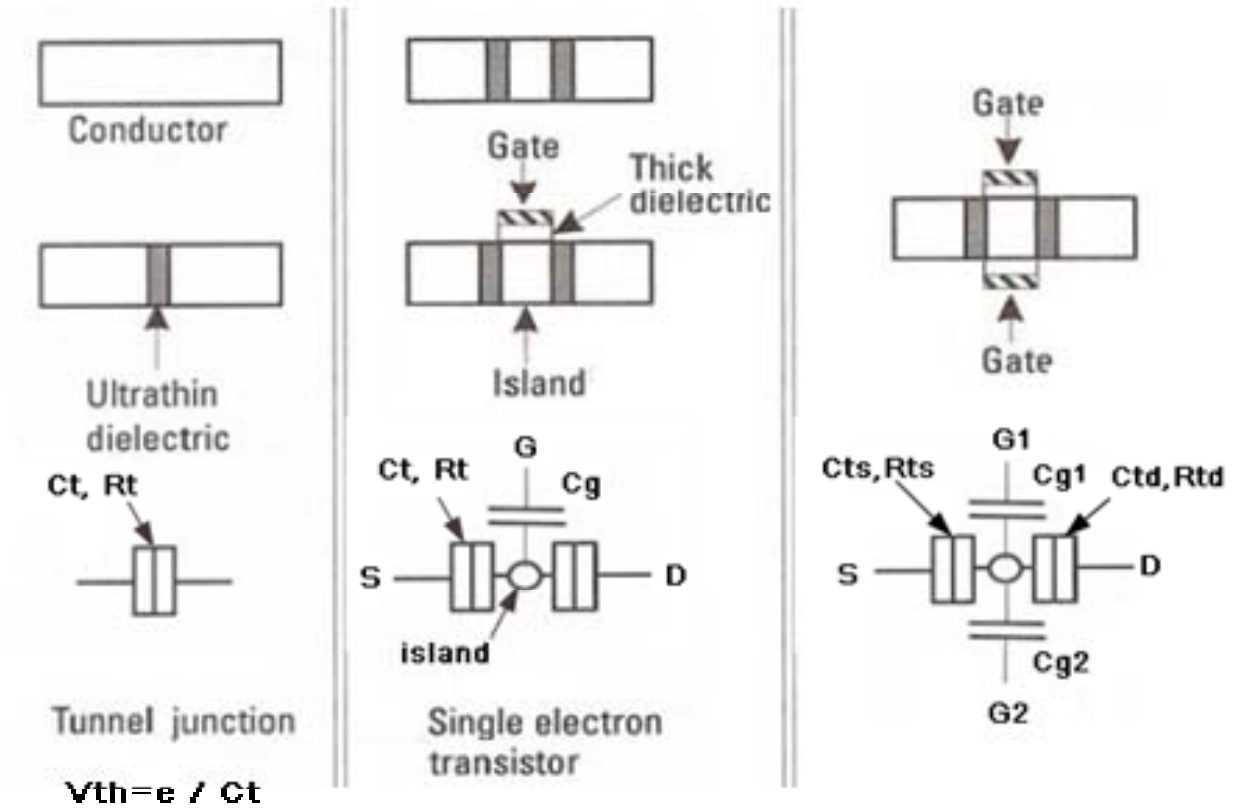
  Advantages:

  - **Nano-scale feature size;**
  - **Ultra-low power dissipation;**
  - **Coulomb Blockade Oscillation;**

SET is more promising for future VLSI design. Its major applications are memory, multiple valued logic, and neural networks.

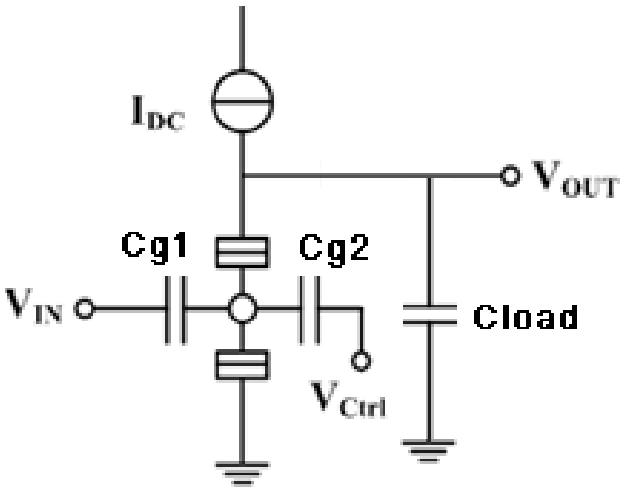
SET transistor and its work principles

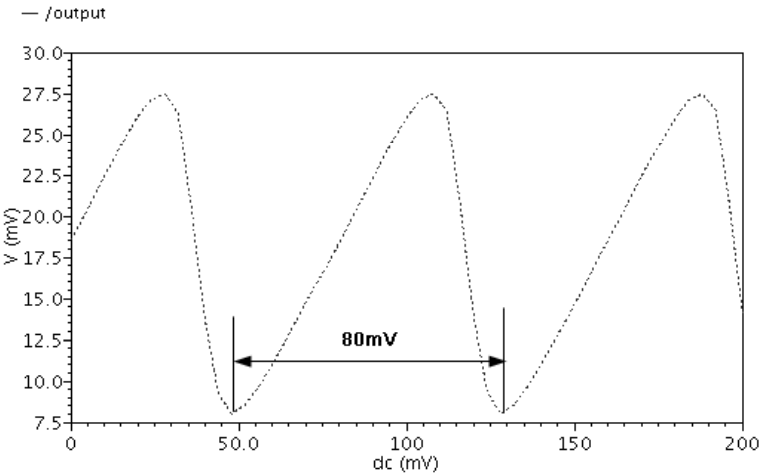
- **SET structure**



SET transistor and its work principles

- **Coulomb Blockade Oscillation**





Parameters: I_{DC} = 2nA; Cg1 = Cg2 = 2aF; Ctd = Ctd =1aF; Rtd = Rts = 1M; Cload = 10fF; T = 10K;

The frequency of the oscillation is e/Cg1 = 80mV.

Why hybrid CMOS-SET circuits

Disadvantages of SET:

- Low current-drivability;
- Small voltage-gain;
- Low-temperature operation;

Advantages of CMOS:

- High-speed current drive;
- High gain;
- Room temperature operation;

It is shown that CMOS devices have advantages that can compensate for the intrinsic drawbacks of SET.

Although a complete replacement of CMOS by single electrics is unlikely in the near future, it is true that by combining SET and CMOS, we can bring out new functionalities which are not mirrored in pure CMOS technology.

Simulation methodology of hybrid CMOS-SET circuits

- **SIMON – SET-based circuit simulator**
  - Most accurate SET circuit simulator.
  - Integrate Monte Carlo method and Master Equations, calculating the probabilities of tunneling events.
  - Time consuming, especially there is current source in the circuit.
  - Not suitable for large scale complex circuits.
  - Cannot co-simulate with MOSFETs.
- **SPICE macro models**
  - Using equivalent circuits based on conventional SPICE components.
  - SPICE compatible and able to co-simulation with MOSFETs.
  - Non-physical and empirical in nature.

Simulation methodology of hybrid CMOS-SET circuits

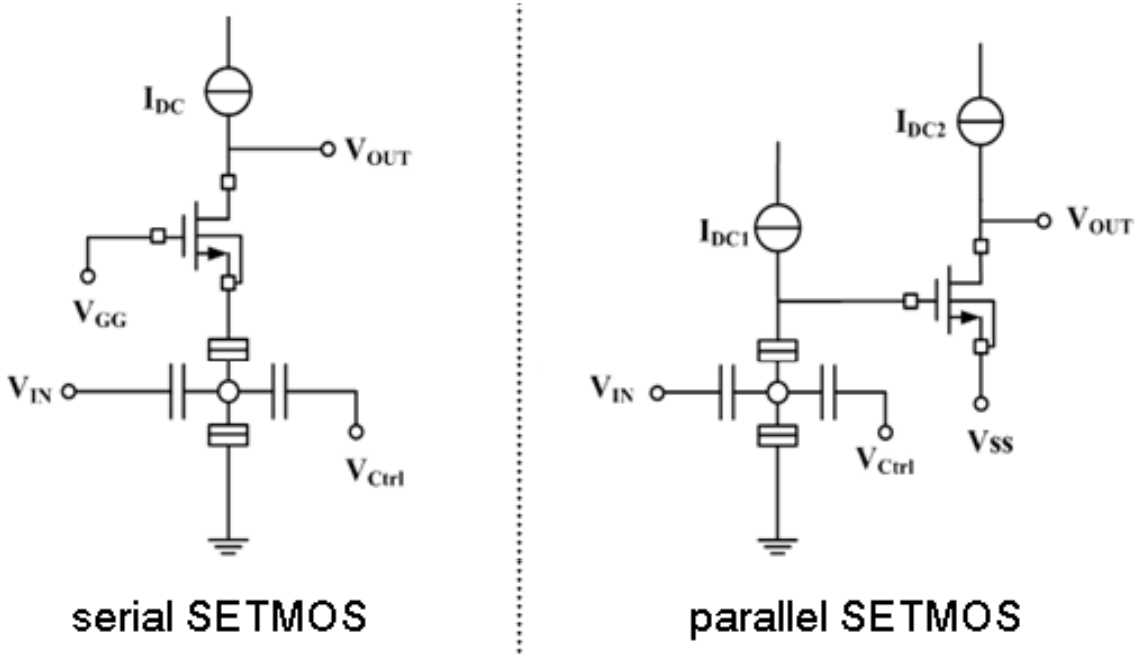
- **MIB compact model**
  - Most accurate model for hybrid CMOS-SET circuit.
  - Using current equations to describe the behavior of SET.
  - SPICE compatible and able to co-simulation with MOSFETs.
  - Integrate thermal components and physical parameters.
  - Developed by AHDL and can be implemented in the SPICE simulator though VerilogA interface.

Assumption:

The interconnect capacitances associated with drain, source and gate terminals of SET are much larger than the device capacitances (that is C_{Σ} = Ctd + Cts + Cg1 +Cg2) which ensures there is no interaction between interconnected SETs.

Two of the most popular hybrid CMOS-SET architectures

- **Serial and parallel SETMOS**



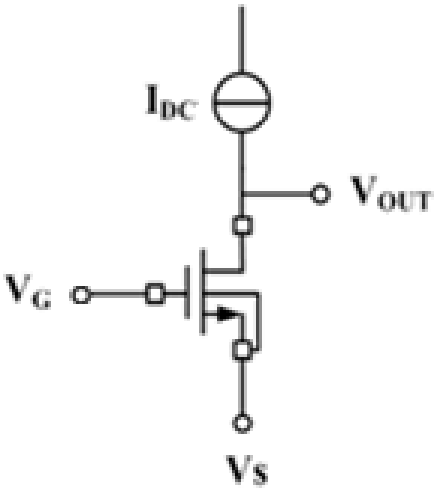
serial SETMOS

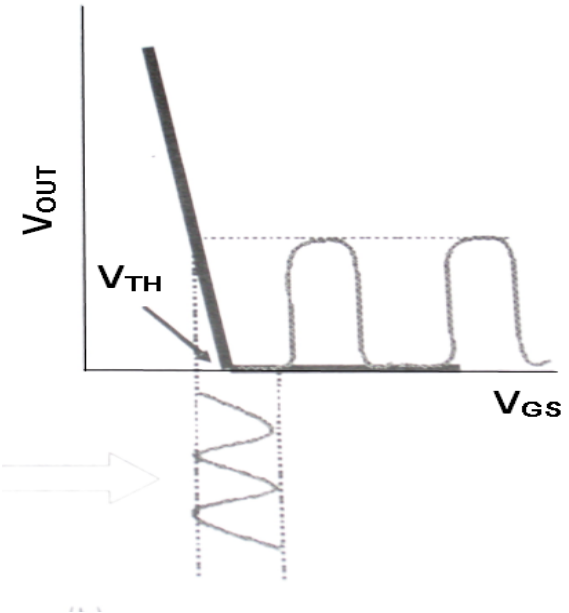
parallel SETMOS

If increasing input voltage of V_{IN} in both architectures, there will be voltage oscillation at drain terminal of SET, and this voltage oscillation can be transferred to the output node.

Two of the most popular hybrid CMOS-SET architectures

- If tuning V_{GG} for serial SETMOS or tuning V_{SS} for parallel SETMOS to bias NMOS transistor in the sub-threshold region, the amplitude of voltage oscillation at drain terminal of SET can be amplified at output node which is suitable for CMOS circuits.





Two of the most popular hybrid CMOS-SET architectures

- **Parameters Selection**
  - For all SETs, Ctd = Cts = 0.1aF; Cg1 = Cg2 = 0.13aF.
  - For all NMOS transistors, W = 500nM; L = 180nM.

Other parameters are shown in the table:

Serial SETMOS	I_{DC}	40 nA
	V_{GG}	655 mV
	V_{Ctrl}	330 mV
Parallel SETMOS	I_{DC1}	40 nA
	I_{DC2}	1 uA
	V_{SS}	–283 mV
	V_{Ctrl}	330 mV

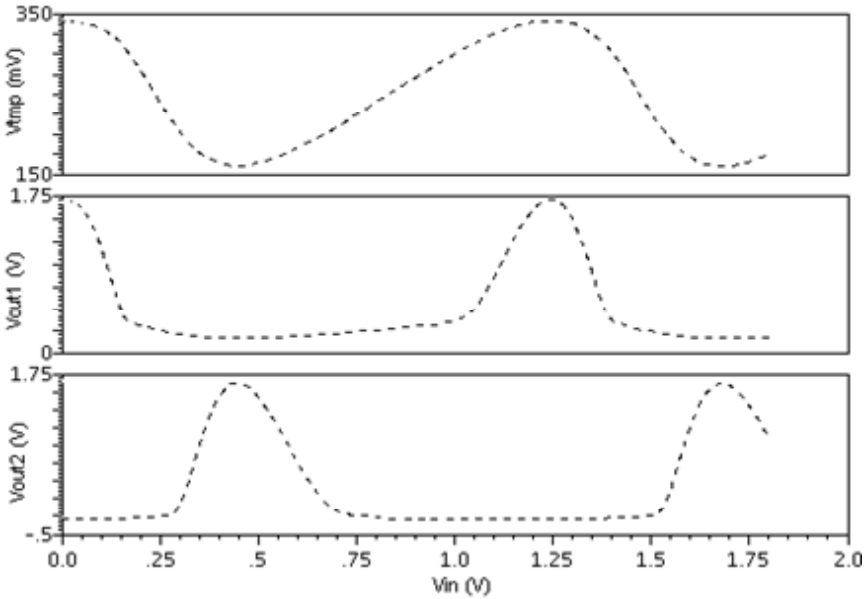
In the following experiments, these parameters will be used otherwise specified.

To ensure the reasonable dynamic range of output voltage oscillation, the value of current connected to the SET cannot be set too large.

V_{Ctrl} is used to adjust the phase of Coulomb blockade oscillation with no effect on the amplitude and frequency of the output.

Two of the most popular hybrid CMOS-SET architectures

- **DC analysis for both serial and parallel SETMOS**
  - Using above parameters and at temperature of 20°C.



•V_{IN} is input voltage changing from 0 to 1.8V.
•Vtmp is the voltage at drain terminal of SET;
•Vout1 is the output voltages of serial SETMOS.
•Vout2 is the output voltages of parallel SETMOS.

It can be seen that the voltage at the outputs of both serial and parallel SETMOS oscillates with amplified magnitude of 1.7V and the periodicity of e/CG1 = 1.25V in the scale of input voltage.

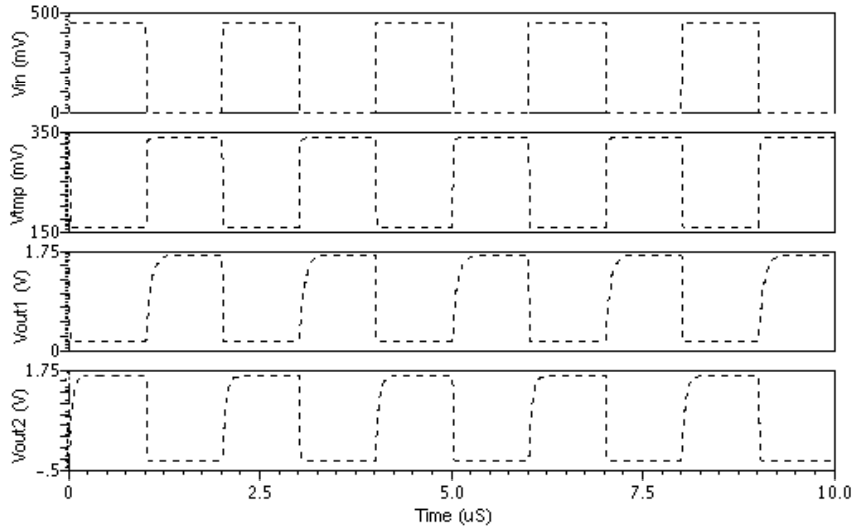
Analysis and compare of serial and parallel SETMOS

- **Power Dissipation**
  - For MOSFETs, the power dissipation is dominated by the dynamic power during logic transition region where there is a current from VDD to ground.
  - For SETs, the most power dissipation is static power at non-transition regions where the output is logic 0 or 1.

  This is because for SET circuits, even though the number of electrons in the island of each SET is constant at the static state, there are still electrons tunneling in and out of the island which contribute to the static power dissipation.

Analysis and compare of serial and parallel SETMOS

- **To calculate the total power dissipation,**
  - Run transient analysis at temperature of 20°C.

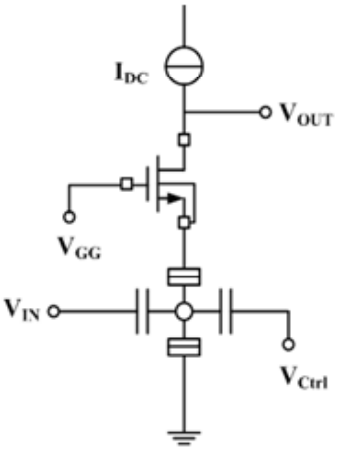


•V_{IN} is ideal clock signal with the voltage swing of 450mV and the period of 2μs.
•Vtmp is the voltage at drain terminal of SET;
•Vout1 is the output voltages of serial SETMOS.
•Vout2 is the output voltages of parallel SETMOS.

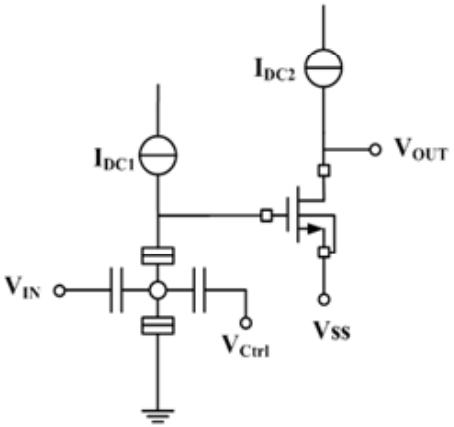
It is shown that serial SETMOS functions as an inverter while the parallel SETMOS acts as a buffer

Analysis and compare of serial and parallel SETMOS

We can calculate power dissipation by integrating output voltage curve, timing with constant current value, and dividing by the period.



serial SETMOS



parallel SETMOS

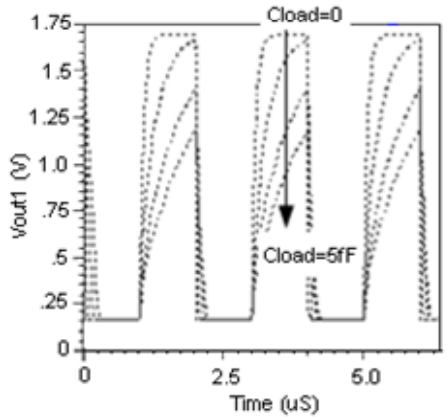
It was found that:

- For serial SETMOS, it has ultra low power dissipation of 35.1nW due to small constant current I_{DC}.
- For parallel SETMOS, however, the total power dissipation turns out to be as high as 676.5nw which is dominated by the power of NMOS transistor (665.5nW).

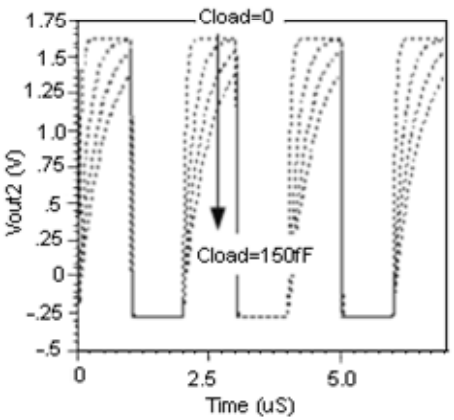
Analysis and compare of serial and parallel SETMOS

- **Drivability**

The drivability of both serial and parallel SETMOS can be tested by adding a load capacitance at the output node.



serial SETMOS



parallel SETMOS

•Run transient analysis at temperature of 20°C with increasing load capacitance.
•Use ideal clock signal with the voltage swing of 450mV and the period of 2μs. as input voltage.

It is shown that:

- For serial SETMOS, it can only drive a capacitive load of several fFs.
- For parallel SETMOS, the drivability is up to several hundreds of fFs.

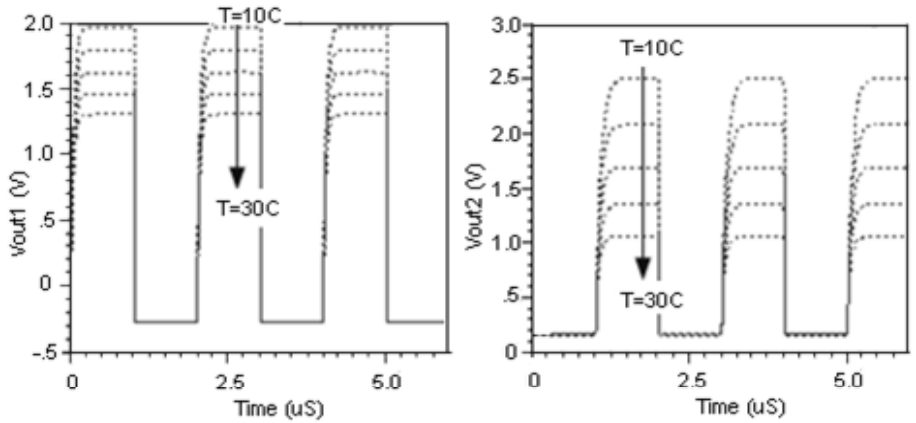
Analysis and compare of serial and parallel SETMOS

- **Temperature Effect**
  - For pure SET circuit, it can only work at extremely low temperature (usually less than 100K). The higher the temperature, the smaller the amplitude of Coulomb Blockade Oscillation.
  - For serial and parallel SETMOS, they can work at much higher temperature if the NMOS transistor is biased to work in the sub-threshold region. This is because the MOSFET has a large voltage gain which can amplify the tiny swing of SET output to an acceptable level.

Analysis and compare of serial and parallel SETMOS

- **Temperature Effect**

  However, both serial and parallel SETMOS are very sensitive to the temperature variation.



serial SETMOS

parallel SETMOS

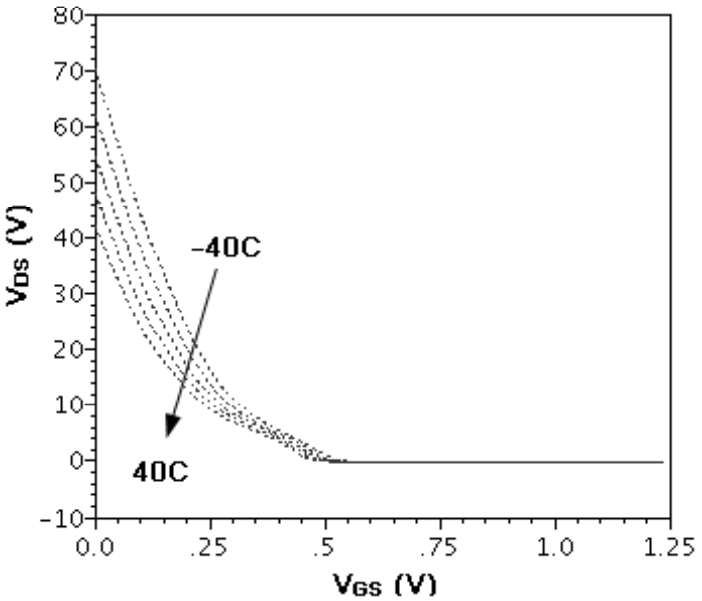
•Run transient analysis with temperature changing from 10°C to 30°C in the step of 5°C.

•Use ideal clock signal with the voltage swing of 450mV and the period of 2μs. as input voltage.

Analysis and compare of serial and parallel SETMOS

- **Temperature Effect**

Temperature	*V_{TH} (mV) with MOS*	*Peak voltage (mV) with SET oscillation*	*Valley voltage (mV) with SET oscillation*
100°C	497.2	312.7	160.1
80°C	509.8	320.1	160.1
60°C	522.3	327.3	160.1
40°C	534.8	334.3	160.1
20°C	545.4	340.9	160.4
0°C	554.1	347.5	160.3
−20°C	562.7	353.7	160.2
−40°C	572.1	359.7	160.4
−60°C	581.1	365.4	160.3
−80°C	588.9	370.5	160.1
−100°C	594.3	375.5	160.1

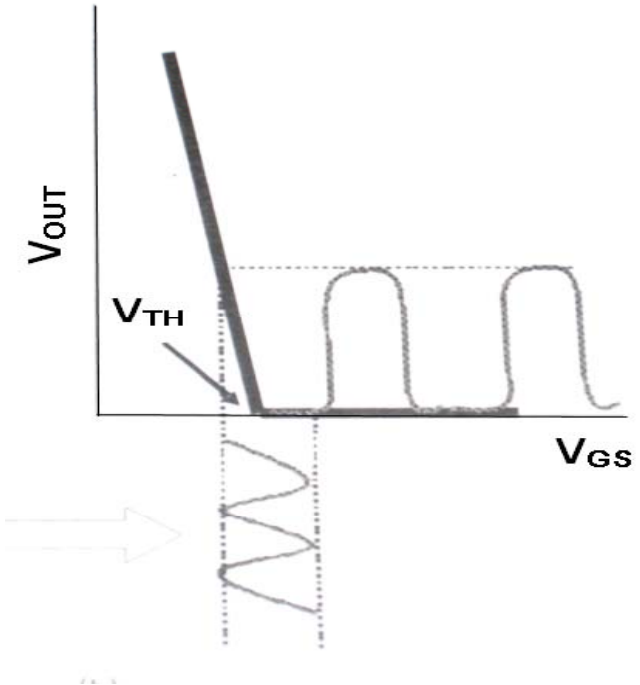


As temperature increases:

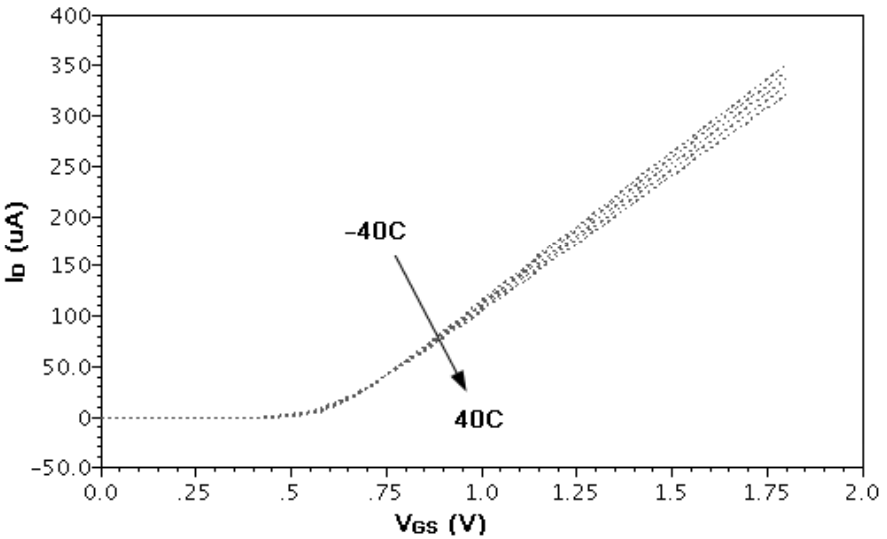
- V_{TH} of NMOS transistor reduces.
- The peak voltage of SET oscillation at the drain terminal of SET reduces.
- The valley voltage of SET oscillation remains almost the same.
- The slope of V_{DS} vs. V_{GS} curve for current-biased NMOS transistor goes down.

Analysis and compare of serial and parallel SETMOS

- **Temperature Effect**

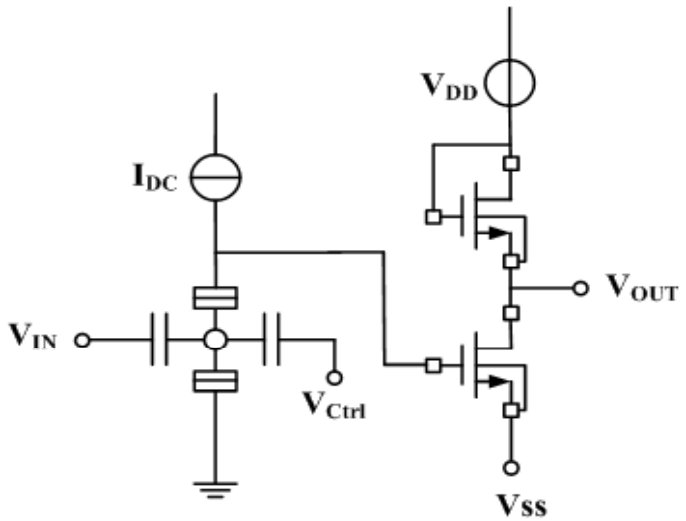


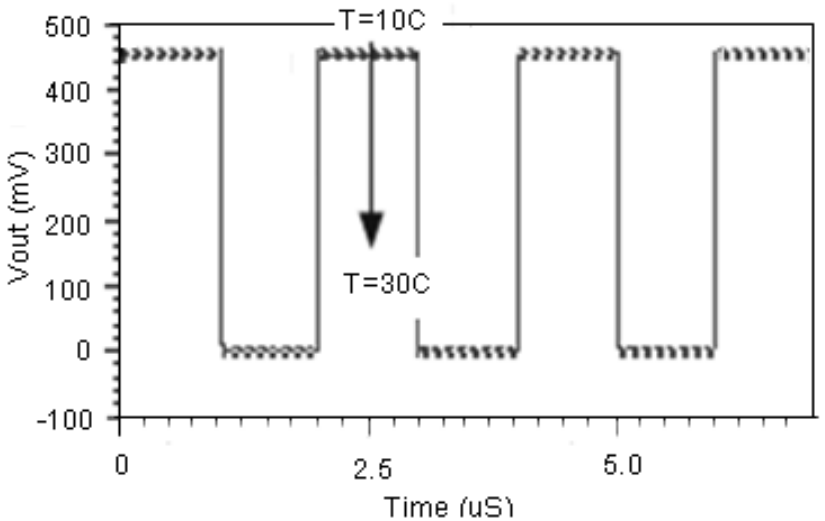
To improve the temperature immunity of hybrid CMOS-SET architectures, the NMOS transistor can be biased by a constant voltage source instead, because for voltage-biased NMOS transistor, the slope of I_D vs. V_{GS} curve is less dependent on temperature



Analysis and compare of serial and parallel SETMOS

- **Voltage-biased parallel SETMOS**
  - Have better temperature performance.
  - Parameters are the same as before except V_{DD} = 1V and $_{VSS}$ = –266mV.
  - The size of extra NMOS transistor is set as W/L = 0.5μm/3.2μm.





Analysis and compare of serial and parallel SETMOS

Summary:

For serial SETMOS:

- Very low power dissipation
- Weak drivability
- Room temperature operation, but much sensitive.

For parallel SETMOS (current-biased):

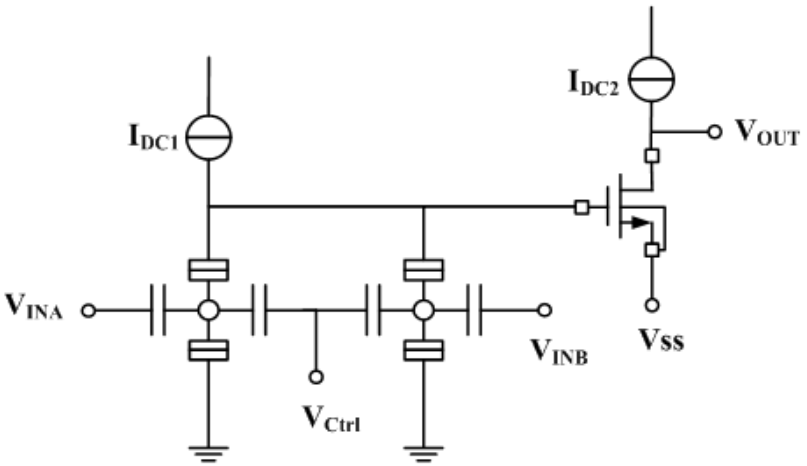
- More power dissipation
- High drivability
- Room temperature operation, but much sensitive.

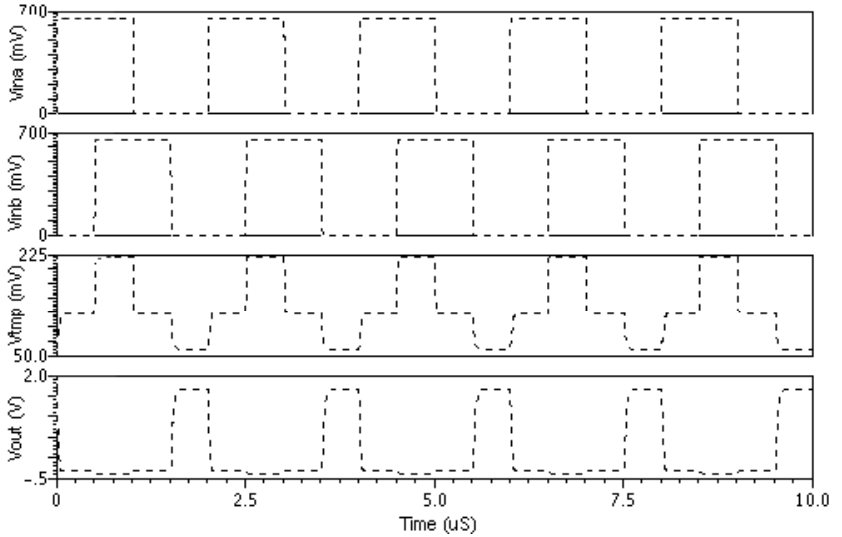
For improved parallel SETMOS (voltage-biased):

- Very large power dissipation
- High drivability
- Room temperature operation, and not sensitive.

Implementation examples using parallel SETMOS architecture

- **Hybrid CMOS-SET NOR gate.**
  - Using parallel SETMOS architecture where I_{DC1} = 30nA, I_{DC2} = 1uA, V_{Ctrl} = 650mV, V_{SS} = –380mV
  - The rest of parameters are the same as before.





Implementation examples using parallel SETMOS architecture

- **Hybrid CMOS-SET NOR gate.**
  - The power dissipation is only 147.6nW in comparison with pure CMOS NOR gate which is several uW.
  - It has very large drivability and can work at room temperature in comparison with pure SET NOR gate which has very low drivability and can only work at extremely low temperature.

  Therefore, the hybrid CMOS-SET NOR gate shares the merits of both CMOS and SET circuits.
- **Hybrid CMOS-SET NAND gate.**

  If NMOS transistor in hybrid CMOS-SET NOR gate is biased by using voltage source and extra NMOS transistor connected in, a hybrid CMOS-SET NAND gate can be realized as well.
  - It has much better temperature performance than hybrid CMOS-SET NOR gate.

Thank You