University of Windsor

2nd M.A.Sc. Seminar :

# Low Power CMOS Rectifier and Chien Search Design for RFID Tags

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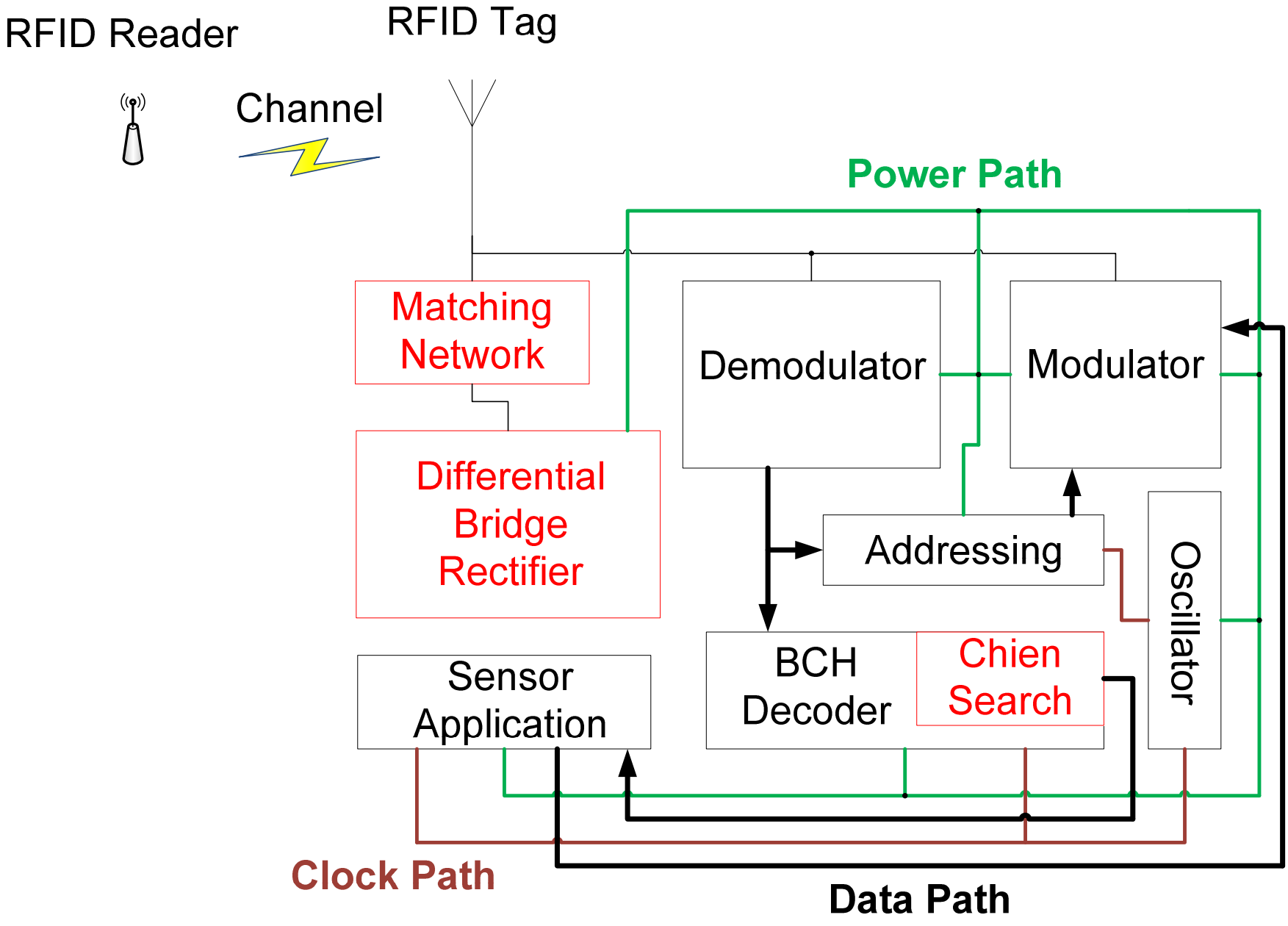
# Introduction

- In noisy automotive environment, Radio Frequency IDentification tags may implement intelligent sensor, which also require extended operating range
- We need robust error correction on the tag and a highly efficient rectifier for power
- BCH code is proven robust and Chien Search is a key part of BCH decoder
- How about differential bridge rectifier?

# Overview of The Seminar

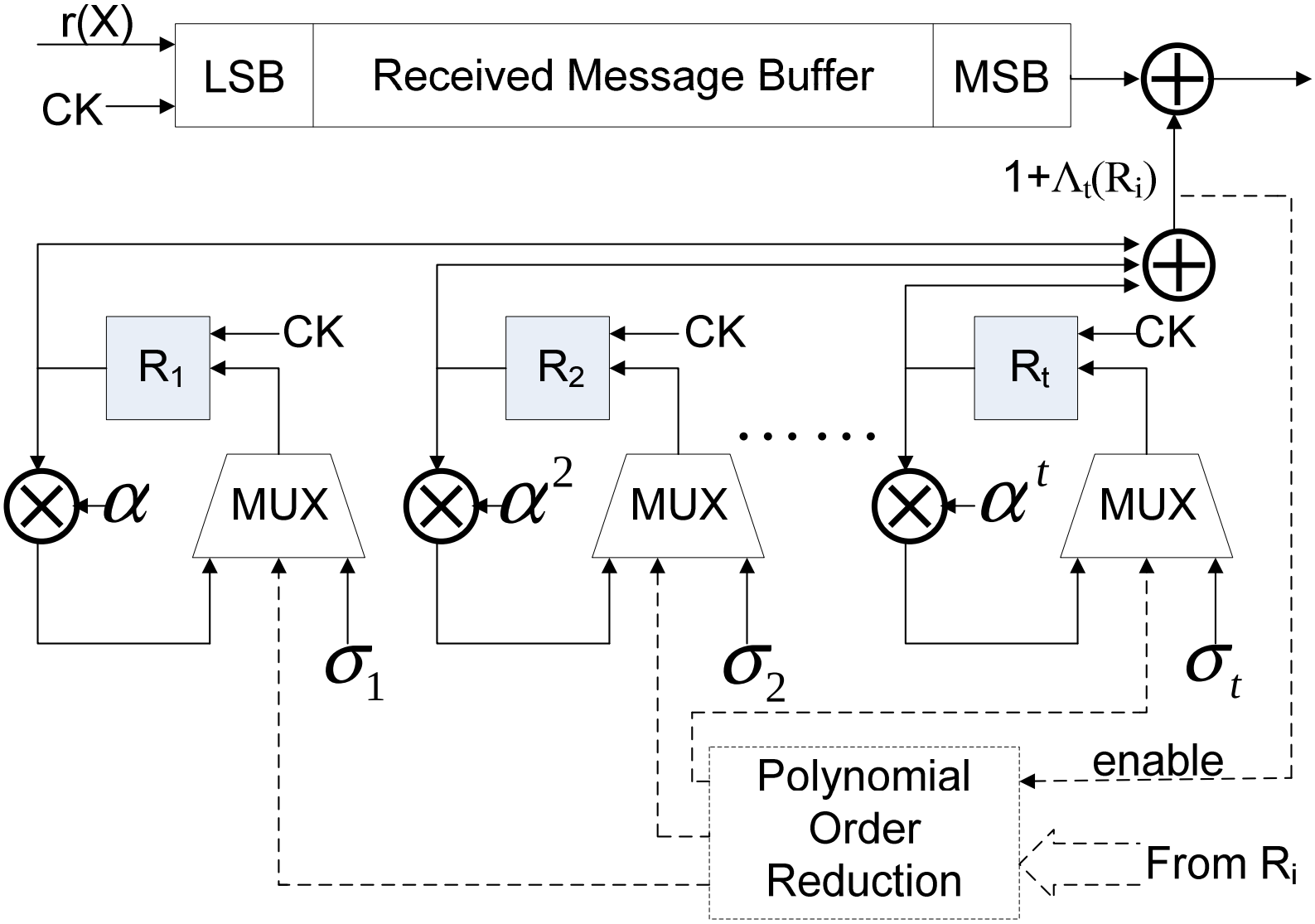
- System overview
- 5 slides for Chien search, which is a key part of my initial research effort
- Introducing differential bridge rectifier
- How to get the highest power efficiency?
- Matching for maximum power transfer?
- Parasitic effects and conclusion

# System Overview

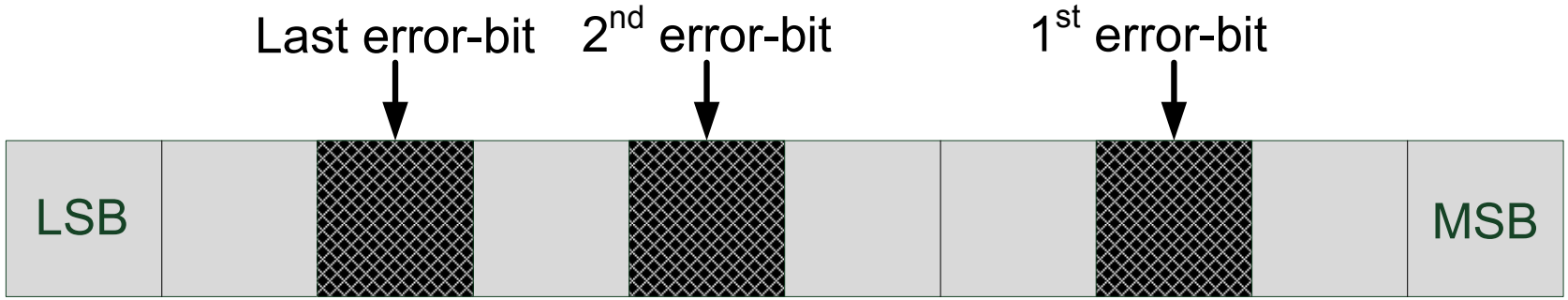


# Chien Search and My Contributions

- Chien search is a popular VLSI circuit for the last decoding step of BCH (Bose-Chaudhuri-Hocquenghem) code, which also consumes the most power
- Proposed a new design strategy for 34% power savings of the circuit
- A paper [1] is published in ISLPED 09
- A journal version is accepted by TVLSI




The conventional Chien Search (solid line) and the Polynomial Order Reduction (dotted line)




Existing Method: [7]

Full power: 8 bit-time
Zero power: 2 bit-time

$$\text{Average power} = \frac{1\times 8 + 0\times 2}{10}$$

$$= 0.8$$

Proposed Method:

Full power: 3 bit-time
2/3 power: 3 bit-time
1/3 power: 2 bit-time
Zero power: 2 bit-time

$$\text{Average power} = \frac{1\times 3 + \frac{2}{3}\times 3 + \frac{1}{3}\times 2 + 0\times 2}{10}$$

$$= \frac{3 + 2 + \frac{2}{3}}{10}$$

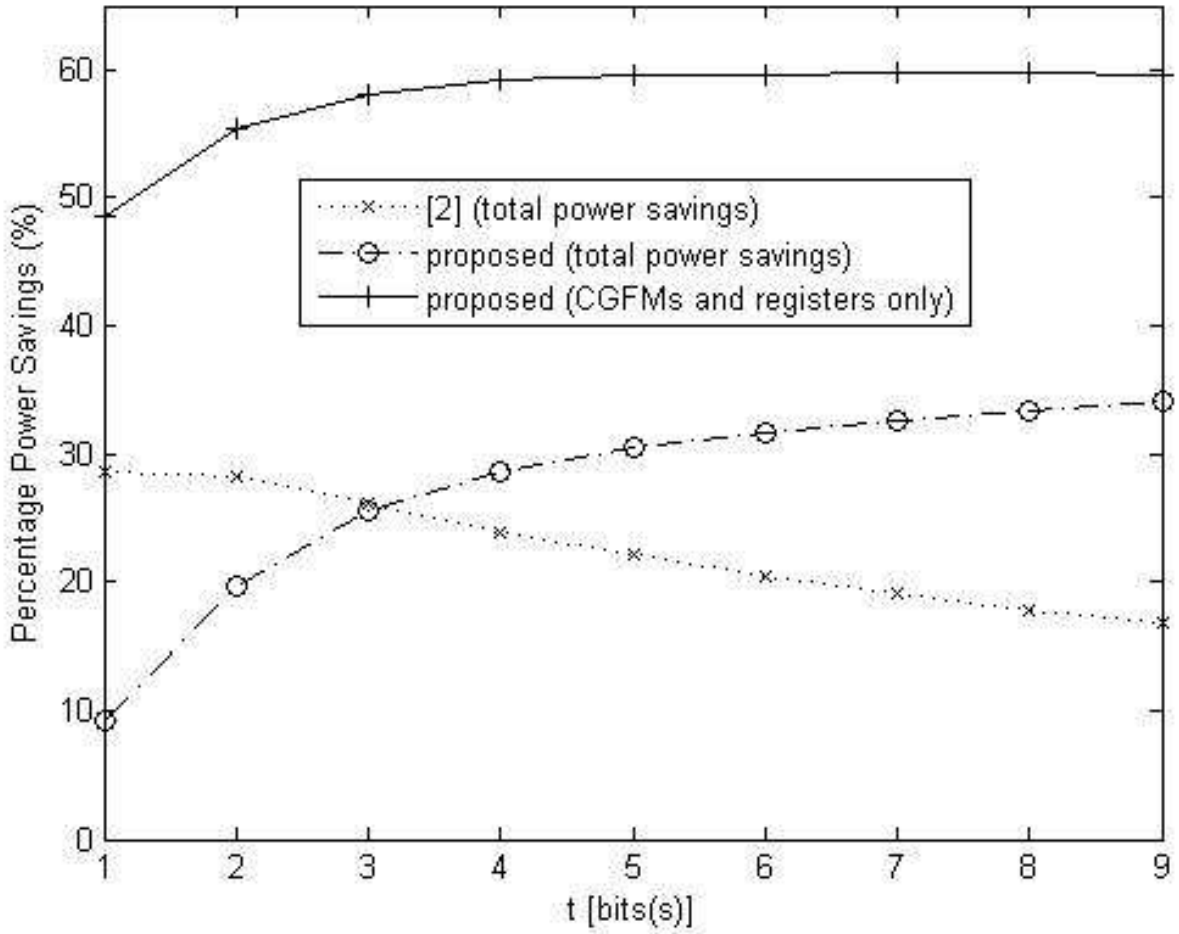
$$= \frac{17}{30}$$

$$= 0.56$$

- Our technique is by first making the constant finite-field multipliers (CGFMs) and registers redundant, through Polynomial Order Reduction (POR) before disabling them via clock gating
- On average, for a ($n$, $k$, $t$) BCH code and $\eta$ = idle/active power for the register, the savings becomes:

$$\overline{S_{prop}} \approx 1 - \left[ \frac{6n}{3n + 2t + 1} \cdot \left( 1 + \frac{t-1}{t+1} \cdot \eta \right) \right]^{-1} \qquad (1)$$

- For POR, with $u$ being the highest order of $\Lambda(R)$, we proved that: $R_w^{'} = \sum_{\lambda=w+1}^{u} R_\lambda$ (2)




- Double the power savings of [2] at $t$=9
- With respect to the conventional circuit, area increase by only 24%, comparing to 106% of the parallel circuit solution [3]

# Prior Work for UHF Rectifier

- Many recent work focus on reducing the turn on threshold voltage of transistor in the Dickson Multiplier topology
- These are such as the External V-th Cancellation method (EVC) [9], the Internal V-th (IVC) [8], Self V-th (SVC) [10] and the Zero V-th transistor (ZVT) [5]
- The maximum Power Conversion Efficiency achieved to date is 37%

# Prior Work for UHF Rectifier ..

- [5] identifies leakage as a PCE bottleneck; power optimization ≠ that of output voltage
- It is commonly assumed that PCE rises with input voltage [6], and [7] proposed boosting the antenna voltage with L-match
- There is an upper limit in voltage boosting due to bandwidth reduction with increasing Q and [6] proposed higher order matching network for maximizing bandwidth

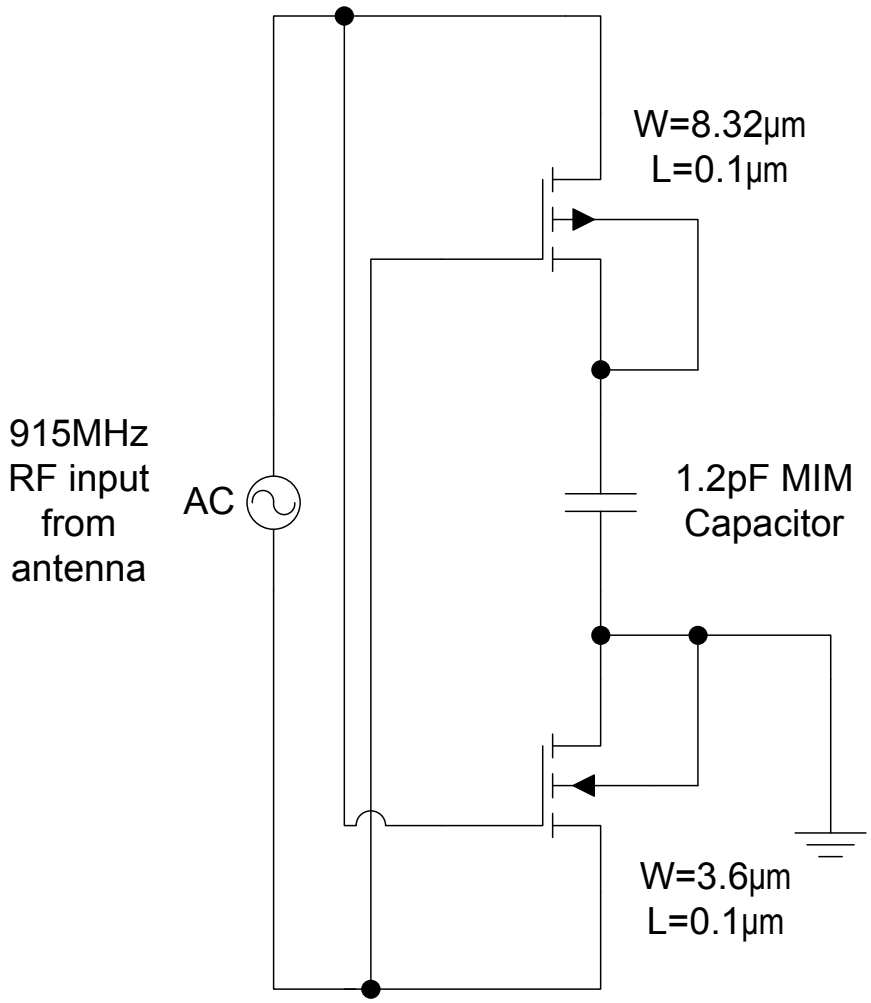
# CMOS Differential Bridge Rectifier

- Implemented in [6] with only PCE of 23%
- Its high PCE potential is rediscovered in 2008 [4]; reported experimental PCE of 66% at input power level of -12dBm
- However, there is no model to support it and it is also not known how a design can be scaled for other load conditions; [4] implies that high PCE is only achievable with high resistance load

# Main Contributions

- A complete 4-D DC analysis of differential bridge rectifier is done with MATLAB, using SPICE model data; The resulting PCE contour shows that there exists a maximum achievable PCE, regardless of the loading, and there is an optimal transistor sizes combination for a given tag distance
- A new design scaling strategy for optimal PCE for all possible loading conditions
- An optimal power matching strategy for non-linear load
- A 3-stages rectifier with simulated PCE of 73% and power utilization of 68% at 10m for 915MHz & $P_{EIRP}$=4W

# CMOS Differential Half-Bridge



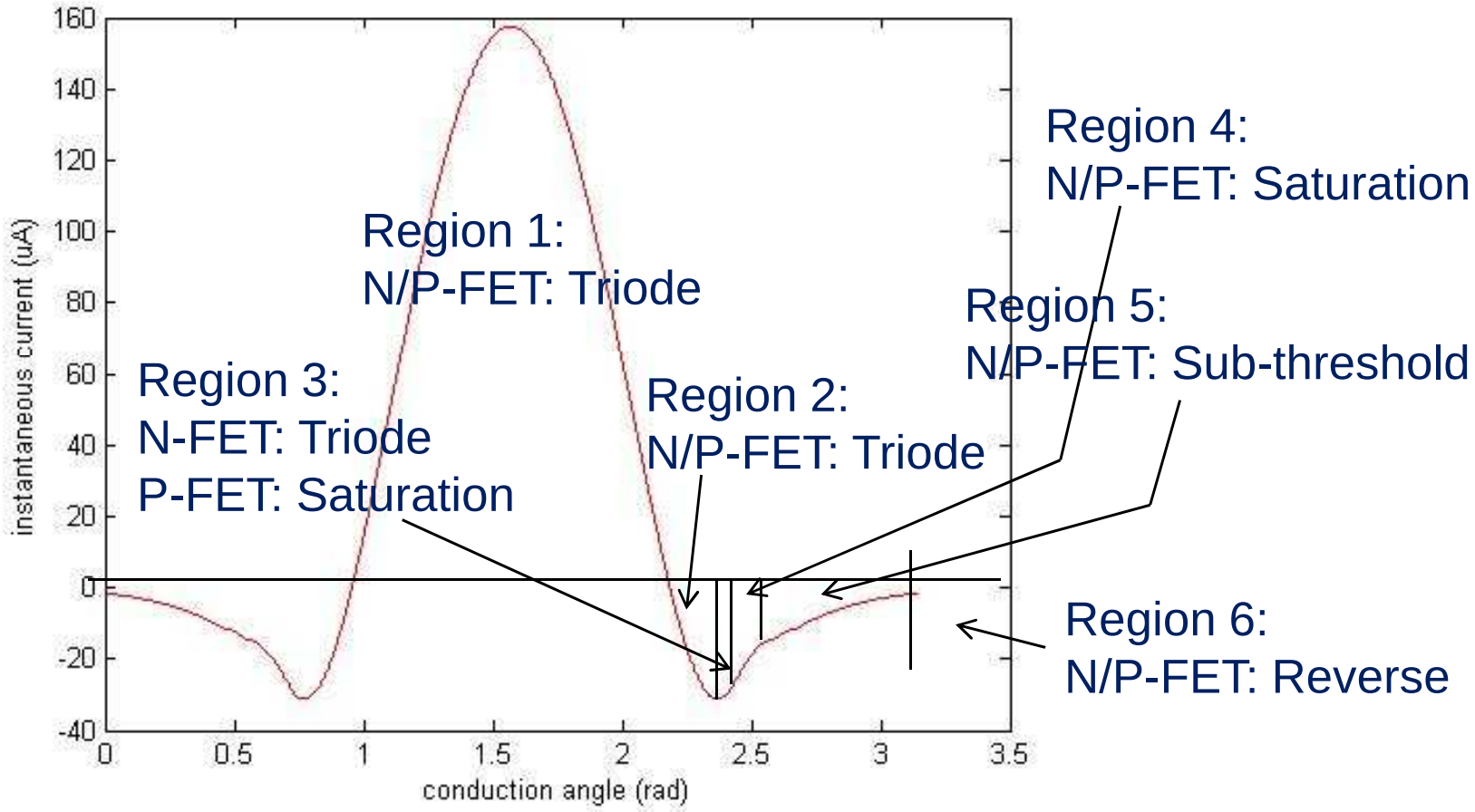

- Operation is rather self explanatory; so, we shall focus only on a few salient pros to the Dickson types
- Input voltage goes fully across Vgs
- No charging cycle
- Parasitic current flows through output

# CMOS Differential Half-Bridge..

- A more detail investigation reveals that when $V_{in} \geq V_{out}$, the current flows from top to bottom; under this condition, $V_{in}=V_{gsp}=V_{gsn}$ and $V_{in}-V_{out}=V_{dsn}+V_{dsp}$ ,therefore:
- $[V_{dsp}, V_{dsn}]<V_{in}-V_{out}$. If we set $V_{out} \geq V_{thp}$, the transistors will turn on in triode mode with small on-resistance!!
- During turnoff when $V_{in}<V_{out}$ , the conditions are more complicated but we can at least notice that $V_{gsn}=V_{out}+V_{dsp}$ , $V_{gsp}=V_{in}-V_{dsp}$, which are decreasing quantities unlike those of the diode-connected FETs used in the Dickson types, which stays constant
- The decreasing Vgs offers a much better turn off

# Six Regions of Conduction

Showing here is a sample current waveform in response to one half cycle of a sinusoidal input

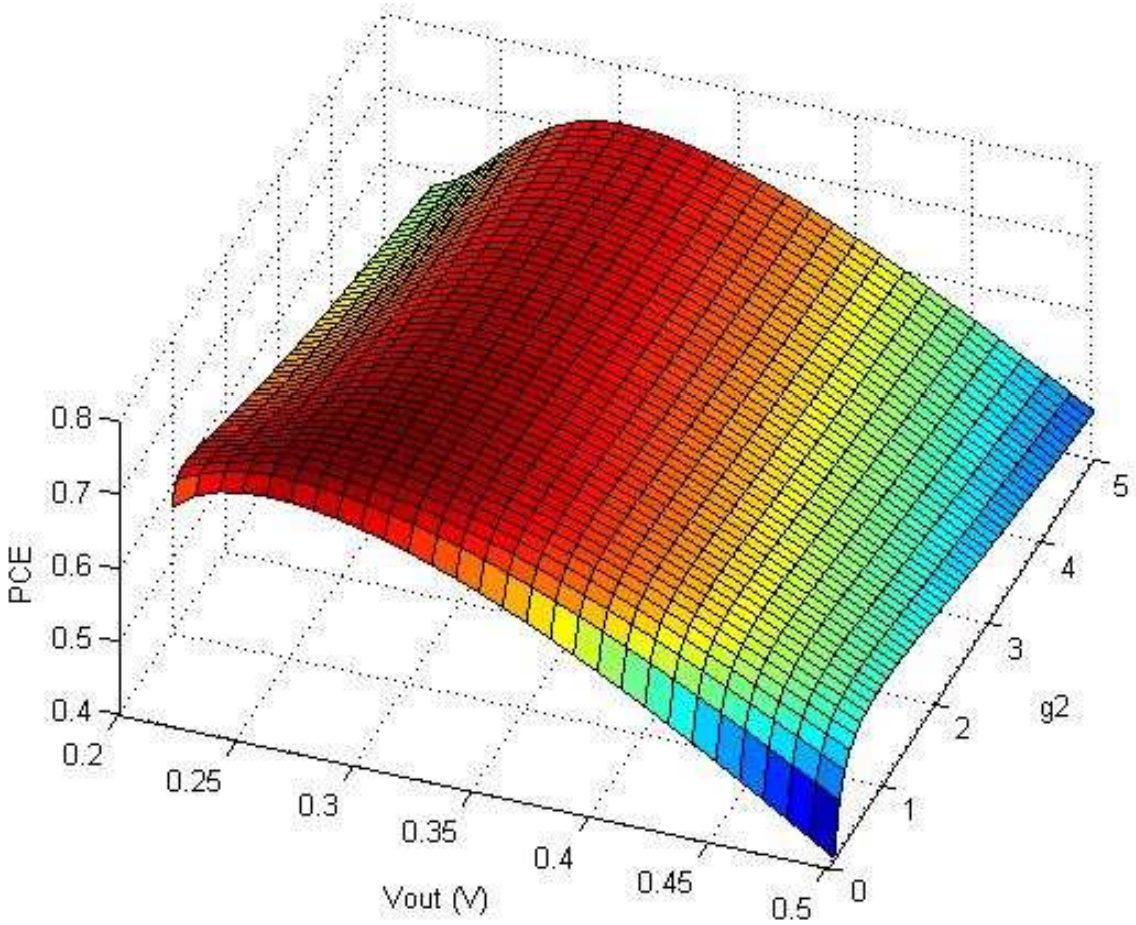



- Analysing details of the reverse conduction regions is vital for the understanding of PCE

# 4-D DC Analysis

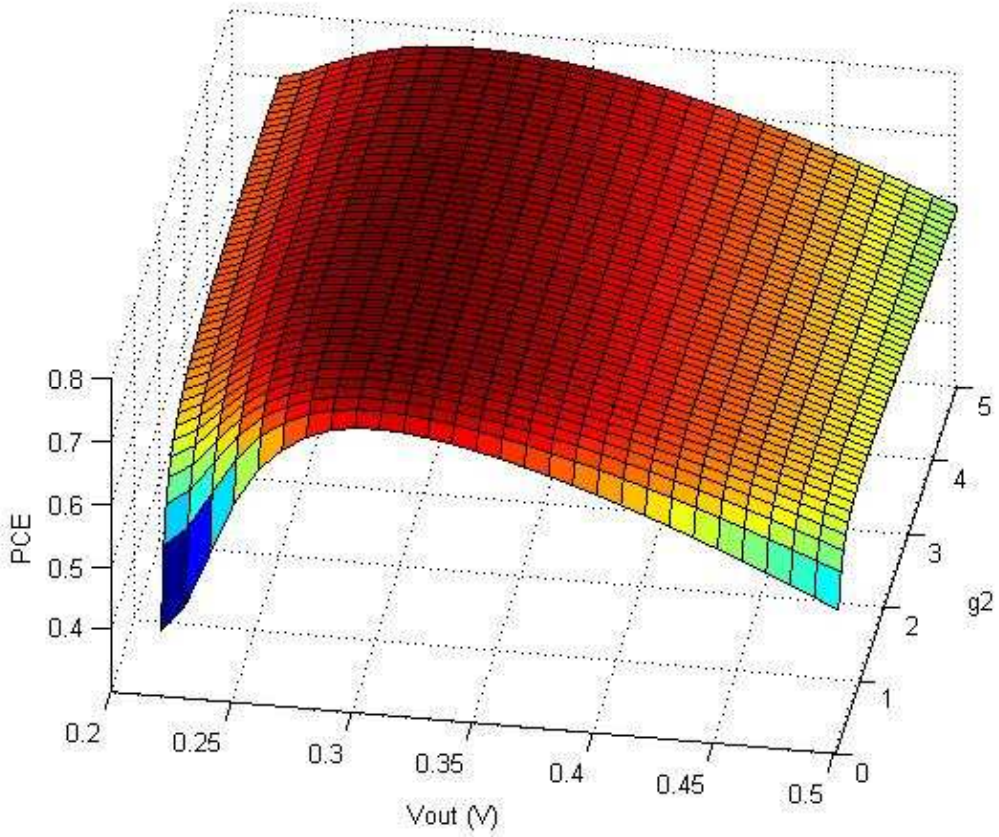
- The reverse regions are generally too complicated for analytical solution
- To discover all possible PCE with any transistor combination, we chose to analyse four parameter dimensions
- PCE, $V_{out}$, $g^2$ ($\beta_p/\beta_n$) and $\delta$ ($V_{out}/V_{in}$)
- This is more than Cadence Spectre can handle, so we wrote a program in MATLAB for the computation

# 3-D PCE contours



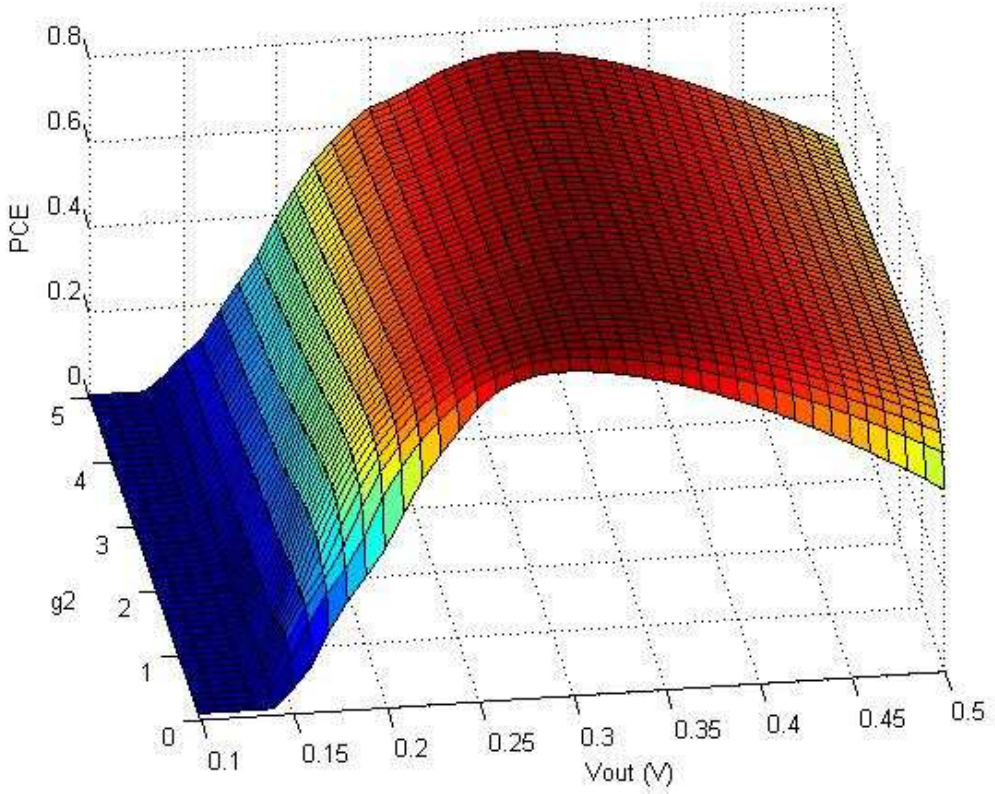

Maximum PCE occurs at an unique point

# Consequence of Body Effect




- Maximum PCE simply shifts to a different point
- Contrary to common assumption, PCE does not decrease but increase !!

# Operating with Low $V_{out}$

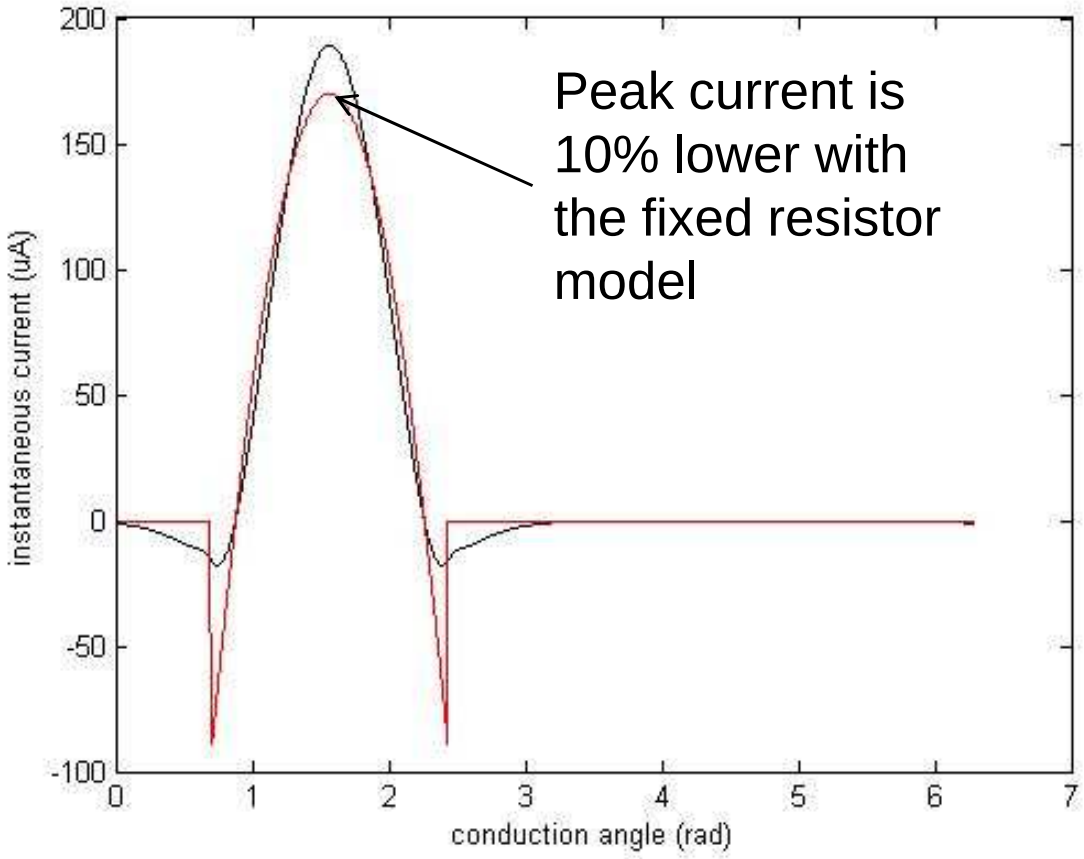



- Setting $V_{out}$ below $V_{thp}$, the threshold voltage of P-type transistor, reduces forward current to a size comparable with the reverse current, resulting in low PCE

# The 4-th Dimension and Summary

- By varying $\delta$, we get a series of different 3-D contours
- A flat contour corresponds to low $\delta$ value and low PCE
- Higher $\delta$ values will yield higher PCEs until a point of diminishing return, where the absolute maximum PCE is located; the relative position of max PCE remains static
- Maximum PCE occurs when $V_{out}$ is slightly above $V_{thp}$
- When $V_{thp}$ is much larger than $V_{thn}$, increasing the relative size of P-type transistor increases PCE
- Given the same $\delta$, higher $V_{sb}$ improves PCE
- When $V_{out}$ is below or much above $V_{thp}$, low PCE results
- Actual PCE will be smaller due to neglected AC effects

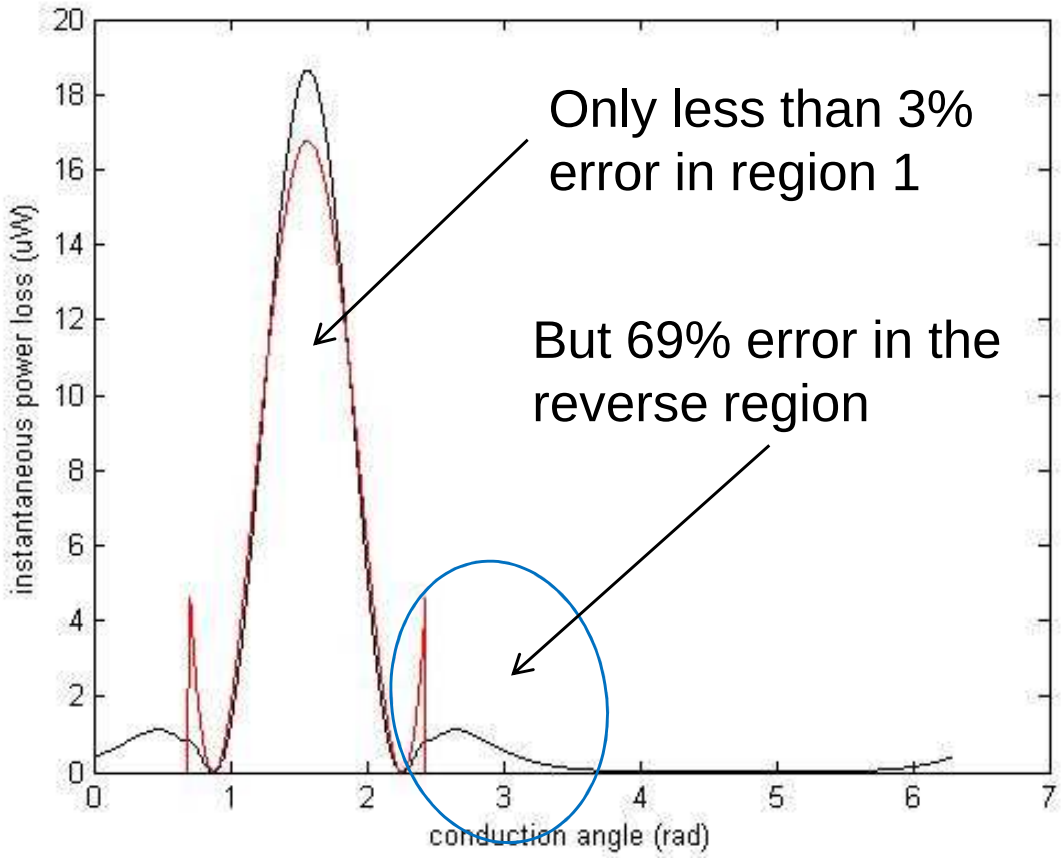
# An Approximated Model



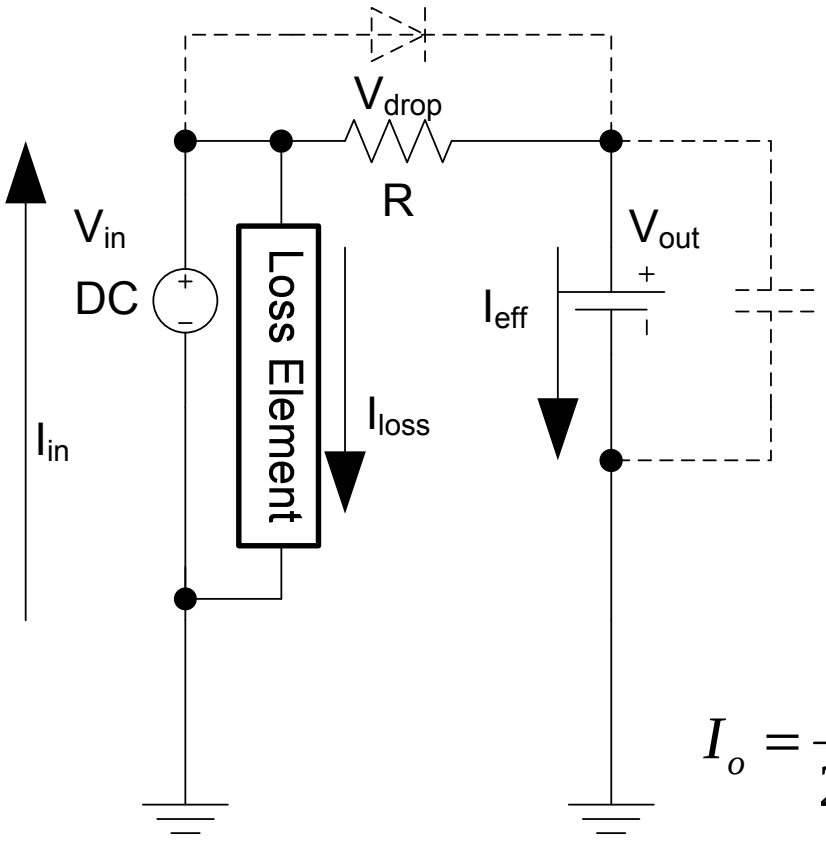

An example for:
$\delta$=0.77
$W_p$=31.35μm
$g^2$=1.4
$V_{out}$=0.33V
$V_{thp}$=0.2785V
$V_{thn}$=0.2806V

This produces an average current of 22.4μA. A resistor that produces the same current has a value of 579.4Ω

- When correctly biased for optimal PCE, the on-region of the transistors behave resistively; could we actually replace it with a fixed value resistor?




- A fixed resistor can sufficiently model region 1
- Since the reverse region loss should be proportional to the forward region loss, we can account for the discrepancy by introducing an equivalent loss resistor

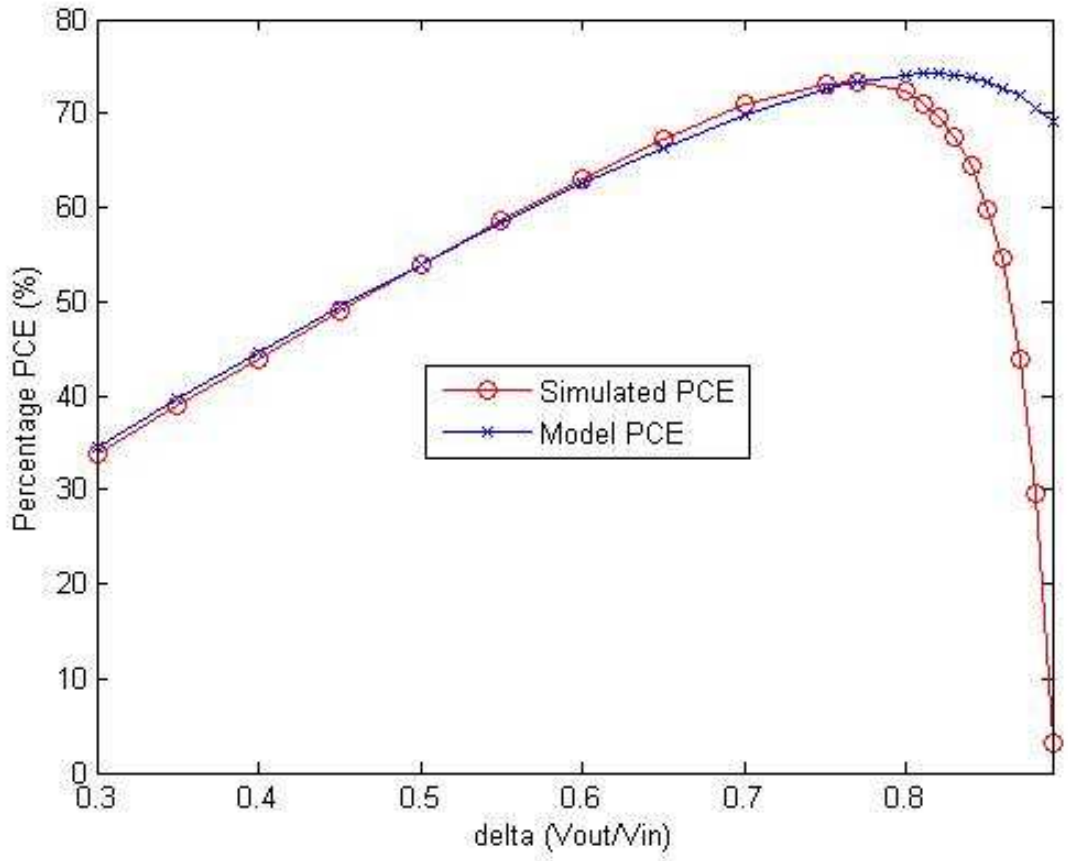



- Assuming a sinusoidal input source, the circuit starts conducting when $V_{in}\cdot\sin(\omega t)>V_{thp}$
- If we further assume that $\delta=V_{out}/V_{in}$ & $\chi=V_{thp}/V_{out}$
- We can show that the average output current $I_o$:

$$I_o = \frac{V_{in}}{2\pi R}\cdot\left[2\sqrt{1-(\chi\delta)^2} - \pi\delta + 2\delta\sin^{-1}(\chi\delta)\right] \quad (3)$$

- We can further derive PCE as follows:

$$PCE = \delta^2 \cdot \frac{\frac{2}{\delta}\sqrt{1-(\chi\delta)^2} - \pi + 2\sin^{-1}(\chi\delta)}{\frac{\pi}{2} - \sin^{-1}(\chi\delta) + \delta\cdot(\chi-2)\cdot\sqrt{1-(\chi\delta)^2} + \frac{\pi R}{R_{loss}}} \quad (4)$$



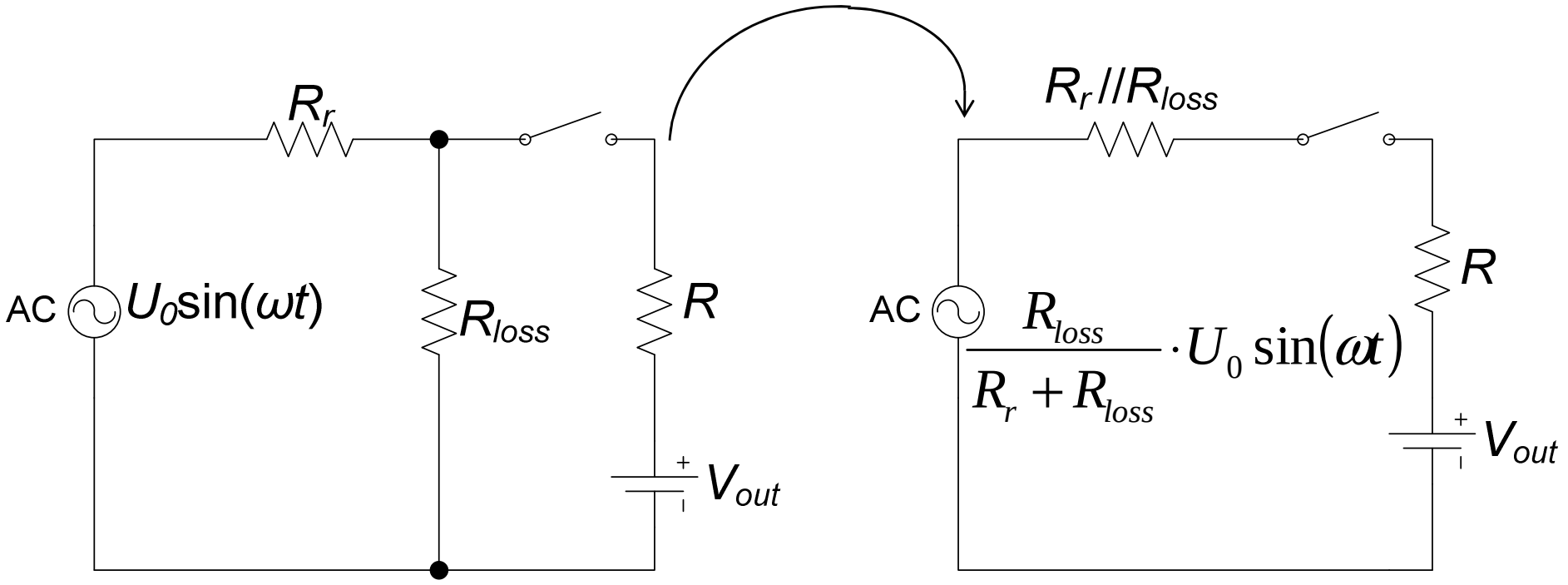

An example for:
$\delta$=0.77
$W_p$=40.2μm
$G^2$=0.6
$V_{out}$=0.33V
$V_{thp}$=0.3117V
$V_{thn}$=0.2237V
$I_o$=33.63μA
*PCE*=73.33%

Effective *R*= 842.8Ω
$R_{loss}$=*135.7KΩ*

- Our model matches the simulated result quite closely up to the maximum PCE of 73.33%
- The model deviates after that point because of the dominance of reverse leakage components

# Matching to Non-Linear Load

- The 4-D PCE contour analysis yields area normalized results, we can scale the transistors for the desired operating current without affecting PCE
- Our model equations are useful for generating $R$ and $R_{loss}$, such that the non-linear rectifier circuit is converted to a piece-wise linear system
- Now, how to match our rectifier to an antenna becomes the issue; prior work assumes a linear model, which is only valid when PCE is low [6]
- But how does it apply to a piece-wise linear system?




- We may model the antenna and the matching network as an AC signal with an amplitude of $U_0$ and an effective radiative impedance of $R_r$; we may further define $k$ and $\sigma$ as the following

$$k = \left(1 + \frac{R_r}{R_{loss}}\right) \cdot \frac{V_{out}}{U_0} \qquad (5)$$

$$\sigma = \frac{R}{R_r // R_{loss}} = \frac{R \cdot (R_r + R_{loss})}{R_r \cdot R_{loss}} \qquad (6)$$

- If $P_r$ is the available power to $V_{out}$, we show that:

$$P_r = \frac{U_0^2}{8R_r} \cdot \left( \frac{R_{loss}}{R_{loss} + R_r} \right) \cdot \frac{8k}{(1+\sigma)\pi} \cdot \left[ \sqrt{1-(\chi k)^2} + k \sin^{-1}(\chi k) - \frac{k\pi}{2} \right] \qquad (7)$$

- The first term is the available power from the antenna, it is related to the distance from reader by Friis equation

$$P_a = \frac{U_0^2}{8R_r} = \frac{P_{EIRP}}{4\pi r^2} \cdot \frac{\lambda^2}{4\pi} \cdot G \qquad (8)$$

wavelength

Antenna gain

$$U_0 = \frac{\lambda}{2\pi r} \sqrt{2P_{EIRP} G R_r} \qquad (9)$$

- So, we can define a power utilization factor PU as:

$$PU = \frac{P_r}{P_a} = \left( \frac{R_{loss}}{R_{loss} + R_r} \right) \cdot \frac{8k}{(1+\sigma)\pi} \left[ \sqrt{1-(\chi k)^2} + k \sin^{-1}(\chi k) - \frac{k\pi}{2} \right] \qquad (10)$$

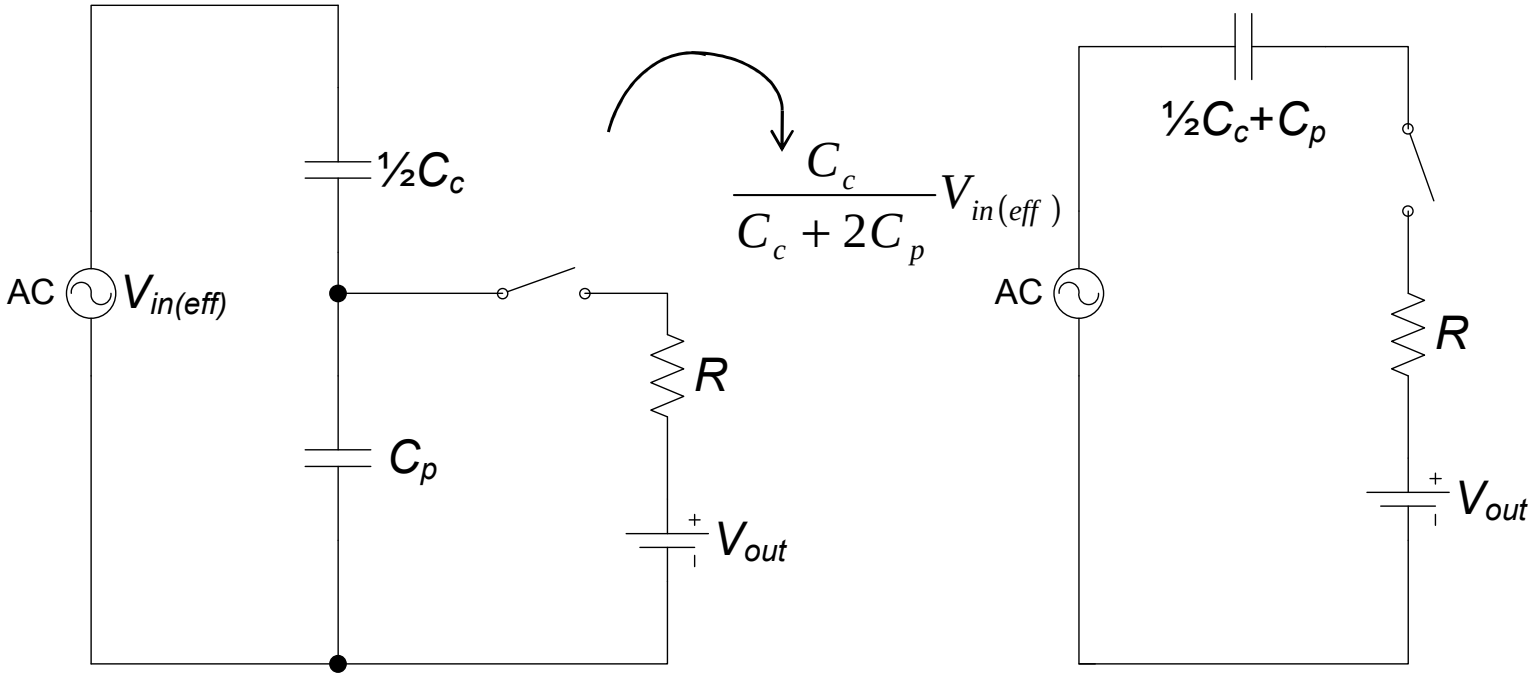
- PU is a function of $k$ and $\chi$, (assuming $R_{loss}$, $R$ and $\sigma$ are known values), differentiating PU($k$) lead to:

$$\frac{dPU(k)}{dk} = \sqrt{1-(\chi k)^2} + 2k\sin^{-1}(\chi k) - k\pi + (1-\chi)\cdot\frac{\chi k^2}{\sqrt{1-(\chi k)^2}} \qquad (11)$$

- maximum power utilization can be founded by setting the equation to zero and then solving it
- For the special case when $\chi$=1, maximum PU for a full-wave bridge rectifier occurs when k=0.3942 at a value of 0.9226
- Therefore, maximum available power to the rectifier's output does not equal $P_a$, but $0.9226P_a$ and it does not occur when $V_{out}$ of each stage is equal to half of the input voltage but:

$$V_{out} = 0.3942\left(\frac{R_{loss}}{R_{loss}+R_r}\right)\cdot U_0 \qquad (12)$$

# Design of Multistage Rectifier




- There is a parasitic capacitance $C_p$ across the load
- And we need coupling capacitor $C_c$ for multistage

- Simple impedance calculation cannot be directly applied as the switching introduces discontinuity
- However, this is nothing more than Laplace transform with some initial conditions at the point of switching; the current through $V_{out}$ is shown to be:

$$i(t) = K_1 \sin(\omega t + \theta + \alpha) + K_2 e^{-\frac{2t}{R\cdot(C_c + 2C_p)}} \qquad (13)$$

- Where: $K_1 = \dfrac{\omega C_c}{\sqrt{4 + \left[\omega R\left(C_c + 2C_p\right)\right]^2}} \cdot V_{in(eff)}$ (14)

$$\alpha = \frac{\pi}{2} - \tan^{-1}\left[\frac{\omega R\left(C_c + 2C_p\right)}{2}\right] \qquad (15)$$

$$\theta = \sin^{-1}\left[\frac{\left(V_{thp} - \Delta V_c\right)\left(C_c + 2C_p\right)}{V_{in(eff)} \cdot C_c}\right] \qquad (16)$$

$$K_2 = \frac{V_{thp} - V_{out}}{R} - K_1 \sin^{-1}\left(\theta + \alpha\right) \qquad (17)$$

- There is charge loss through the equivalent capacitor during the switching that occurs on every cycle, these charge loss caused a voltage drop $V_{dt}$

$$V_{dt} = \frac{I_{load\,(total)}}{f \cdot \left(C_c + 2C_p\right)} \qquad (18)$$

- For fullwave rectifier, during steady state, the initial voltage at the capacitor becomes:

$$\Delta V_c = \frac{V_{dt}}{2} \qquad (19)$$

- Which means although there is a voltage drop, the initial DC offset keeps the amplitude of the signal seen by *R* and $V_{out}$ almost exactly the same before and after switching; there is only a phase shift involved

- The current through $C_c$ can be found from $i(t)$, which could then be used for determining the effective $V_{out}$
- The effective $R$ can be calculated by recognizing the tap-capacitor matching circuit

$$R_{eff} = \frac{1+Q^2}{1+Q_2^2}\left(R \,//\, R_{loss}\right) \qquad (20)$$

$$Q_2 = \omega C_p \left(R_{loss} \,//\, R\right) \qquad (21)$$

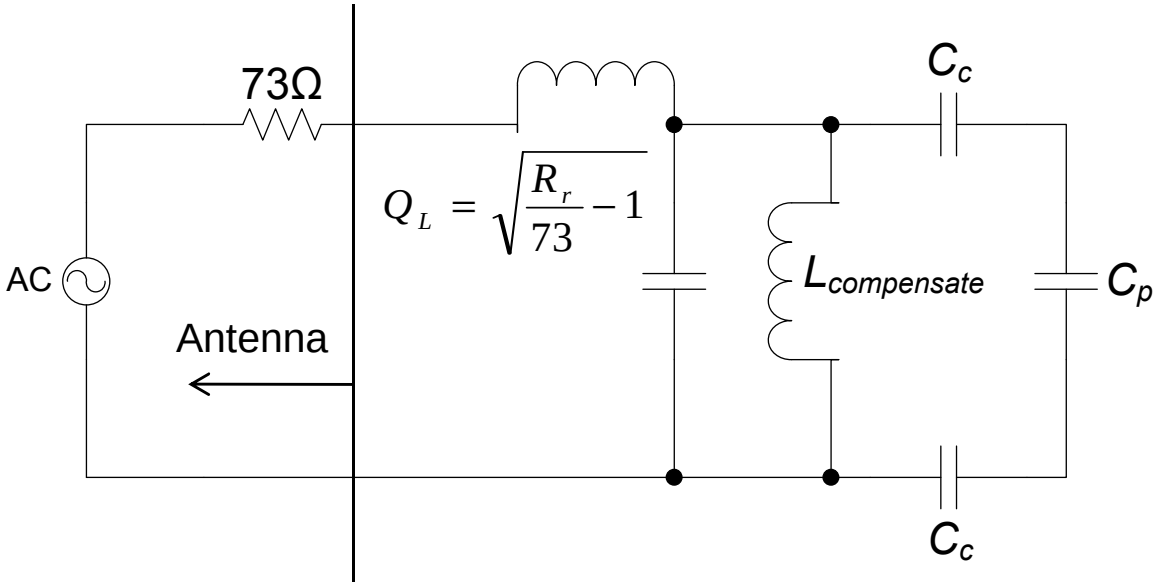
$$Q = \frac{1}{\left[\frac{1}{2}C_c \,//\left(\frac{1+Q_2^2}{Q_2^2}C_p\right)\right]\cdot\frac{R \,//\, R_{loss}}{1+Q_2^2}\cdot\omega} \qquad (22)$$

- The reactive current due to $C_c$ and $C_p$ can be cancelled with an in-parallel inductor; the low Q due to the poly-silicon gates can be relieved by multiple fingers
- Finally, we need to determine the required $R_r$

- It can be shown that:

$$\sigma = \frac{k(1-\delta)}{\delta - k} \qquad (23) \qquad R_r = \frac{R_{eff} \cdot R_{loss}}{\sigma \cdot R_{loss} - R_{eff}} \qquad (24)$$

- Typically, low cost antenna has simple design with low impedance, such as dipole antenna with an impedance of 73Ω; L-match may be used to convert 73Ω to $R_r$




- Maximum power utilization rules imply that effective $V_{out}$ for each stage should be the same

- Since $V_{out}$ also fixes $U_0$, it implies maximum PU only at one distance. Reversely speaking, it means that, for any given distance, there exists an optimal transistor size
- With these design rules, we came up with a 3-stages full-wave differential bridge rectifier circuit, results follows:

| r(m) | Pa (μW) | Pa (dBm) | PU | PCE | Io (μA) |
|---|---|---|---|---|---|
| 5 | 178.38 | -7.49 | 0.6399 | 0.6982 | 115.3 |
| 7 | 91.01 | -10.41 | 0.7174 | 0.7267 | 65.95 |
| 9 | 55.06 | -12.59 | 0.7099 | 0.7405 | 39.48 |
| 10 | 44.59 | -13.51 | 0.6795 | 0.7382 | 30.61 |
| 11 | 36.86 | -14.34 | 0.6294 | 0.7336 | 23.43 |
| 12 | 30.97 | -15.09 | 0.5626 | 0.7165 | 17.6 |
| 13 | 26.39 | -15.79 | 0.4806 | 0.6851 | 12.81 |

# Conclusions

- Developed a complete design methodology for differential bridge rectifier
- Shown that a different optimal power transfer equation applies to this rectifier
- Shown that there is an optimal transistor size for a target distance
- And that body-effect and high output current will not necessarily degrade PCE
- Simulated a design with PCE of 73% & PU of 67% at 10m and $P_{EIRP}$ of 4W

# Reference


1. S.Wong, C.Chen, Q.M.J. Wu, “Power-Management-Based Chien Search for Low Power BCH Decoder,” International Symposium on Low Power Electronics and Design, 2009, ISLPED 2009, Aug 19-21, 2009
2. Y. Wu, “Low power decoding of BCH codes,” IEEE International Symposium on Circuits and Systems, ISCAS 2004, vol. 2, May 2004, pp. II-369-372.
3. A. Raghupathy and K. J. R. Liu, “Algorithm-based low-power/high-speed Reed-Solomon decoder design,” IEEE Trans. on Circuits and Systems—II: Analog and Digital Signal Processing, vol. 47, no. 11, Nov. 2000, pp. 1254-1270.
4. A. Sasaki, K. Kotani, T. Ito, “Differential-Drive CMOS Rectifier for UHF RFIDs with 66% PCE at -12dBm Input,” IEEE Asian Solid-State Circuits Conference, 2008, A_SSCC’08, 3-5 Nov, 2008, pp. 105-108
5. J. Yi, W. Ki, C. Tsui, “Analysis and Design Strategy of UHF Micro-Power CMOS Rectifiers for Micro-Sensor and RFID Applications”, IEEE Trans. on Circuits and Systems-I: Regular Papers, Vol. 54, No.1, January 2007, pp.153-166

6. S. Mandal, R. Sarpeshkar, “Low-Power CMOS Rectifier Design for RFID Applications”, IEEE Trans. on Circuits and Systems-I:Regular Papers, Vol. 54, No.6, June 2007, pp. 1177-1188
7. A. Shameli, A. Safarian, A. Rofougaran, et al., “Power Harvester Design for Passive UHF RFID Tag Using a Voltage Boosting Technique”, IEEE Trans. on Microwave Theory and Techniques, Vol. 55, Issue 6, Part 1, June 2007, pp.1089-1097
8. H. Nakamoto, D. Yamazaki, T. Yamamoto, H. Kurata, S. Yamada, K. Mukaida et al., “A Passive UHF RF Identification CMOS Tag IC Using Ferroelectric RAM in 0.35-μm Technology”, IEEE Journal of Solid-State Circuits, Vol. 42, No.1, January 2007, pp. 101-110
9. T. Umeda, H. Yoshida, S. Sekine, Y.Fujita, et al., “A 950-MHz Rectifier Circuit for Sensor Network Tags With 10-m Distance”, IEEE Journal of Solid-State Circuits, Vol. 41, No. 1, January 2006, pp. 35-41
10. K. Kotani, T. Ito, “High Efficiency CMOS Rectifier Circuit with Self-Vth-Cancellation and Power Regulation Functions for UHF RFIDs”, IEEE Asian Solid-State Circuits Conference 2007, ASSCC 07, Nov. 07, pp. 119-122
11. C. Ma, C. Zhang, Z. Wang, “Power Analysis for the MOS AC/DC Rectifier of Passive RFID Transponders”, IEEE Asia Pacific Conference on Circuits and Systems 2006, APCCAS 2006, Dec. 06, pp.1350-1353

# Endorsements

- These work were funded by the AUTO21 Network of Centres of Excellence, Canada

Questions?