A 12-b 30-MS/s, Low-Power, Low-Area Pipelined A/D Converter Using Voltage-Mode and Current-Mode Stages

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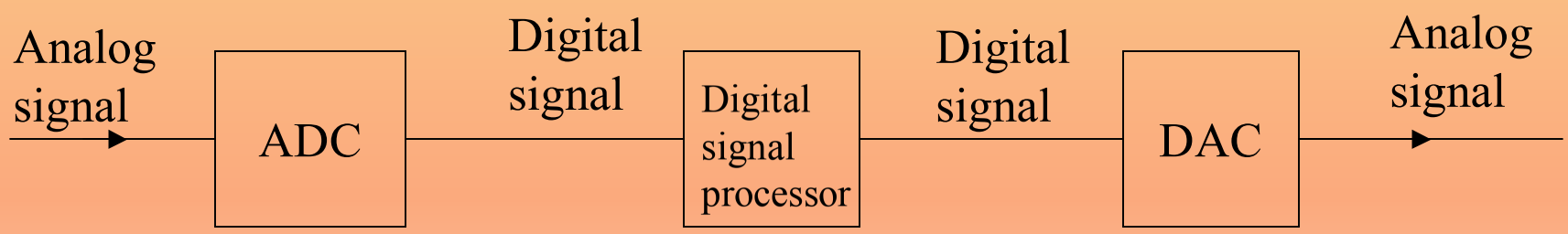
Introduction:

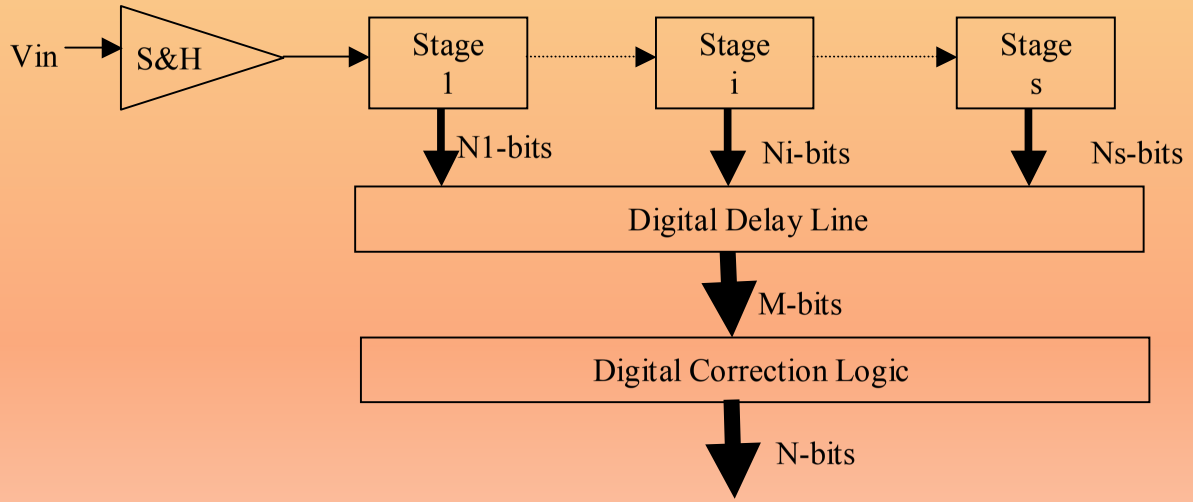
A/D converters are the interface between analog circuits and digital circuits.
Examples:
High-Definition Television, Multimedia, Wireless communication, Radar systems, Modems, Control systems and etc...



Digital Signal Processing

Conventional Architecture of Pipelined ADC

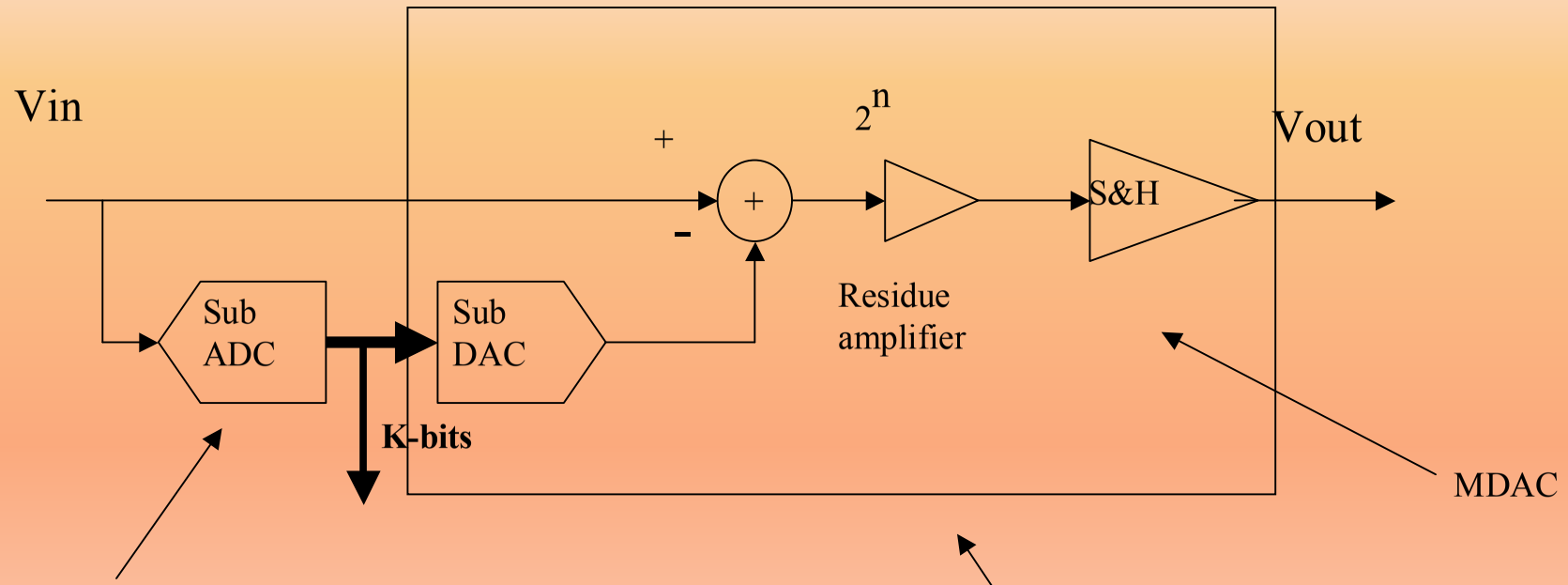
The input is sampled and held, the first stage processes the sampled signal and produces digital outputs and the analog output. The digital output is stored in digital delay line and analog output is processed by the second stage. While the second stage is processing the analog output of the previous stage, the previous stage is processing a new sample.



Advantages: High speed, Low area and low power dissipation.

Applications: Battery powered devices, Video processing, cable modem, Asymmetrical digital subscriber line(ADSL). 1MHZ-100MHZ, 8-16 bits.

Generic Architecture of one Stage



Low-Resolution
Flash Quantizer

Multiplying Analog-to-Digital
Converter (MDAC)

Pipelined Stages Circuit Design

A) Fully Differential Voltage Mode (Conventional)

Advantages: High accuracy, High speed.

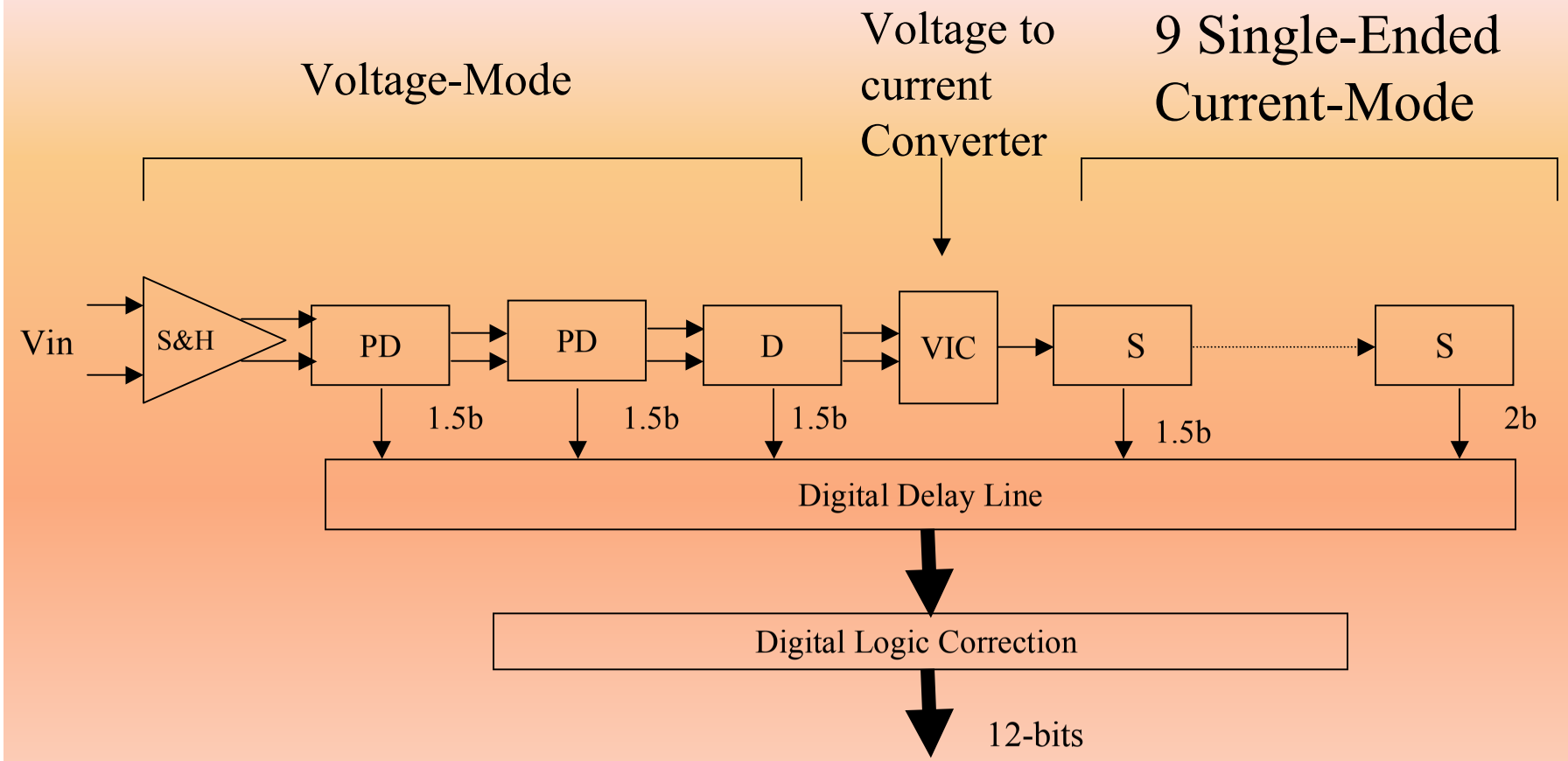
Disadvantages: Requires High gain, fast settling time Op-amps Which requires large biasing current therefore high power dissipation. Requires large and linear capacitors which consume large area.

B) Current Mode:

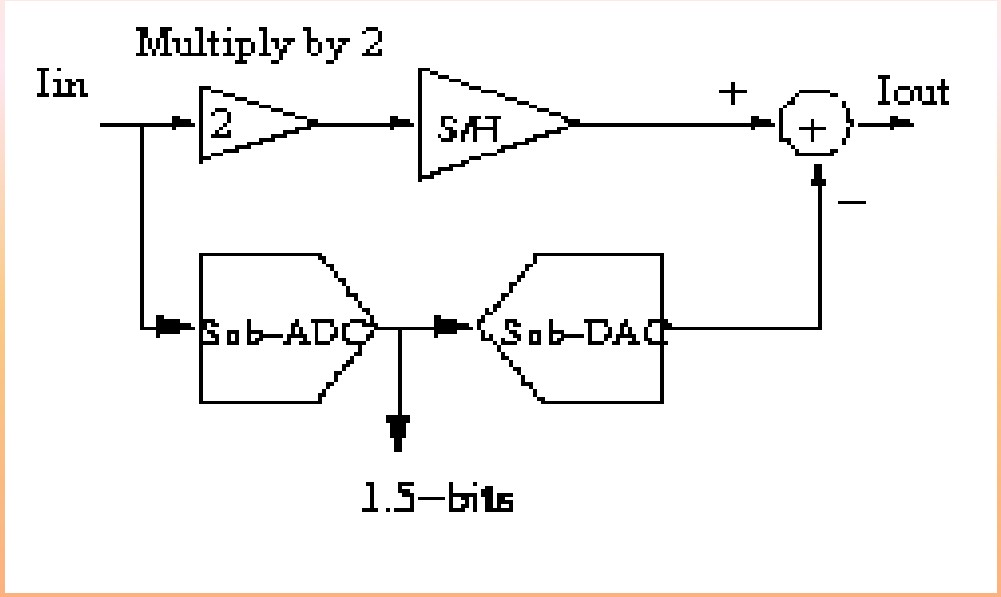
Advantages: No large and accurate capacitors needed. No op-amp with large biasing current needed there Less power dissipation and area.

Disadvantage: Less accuracy

Proposed Architecture



Current Mode Stages Architecture

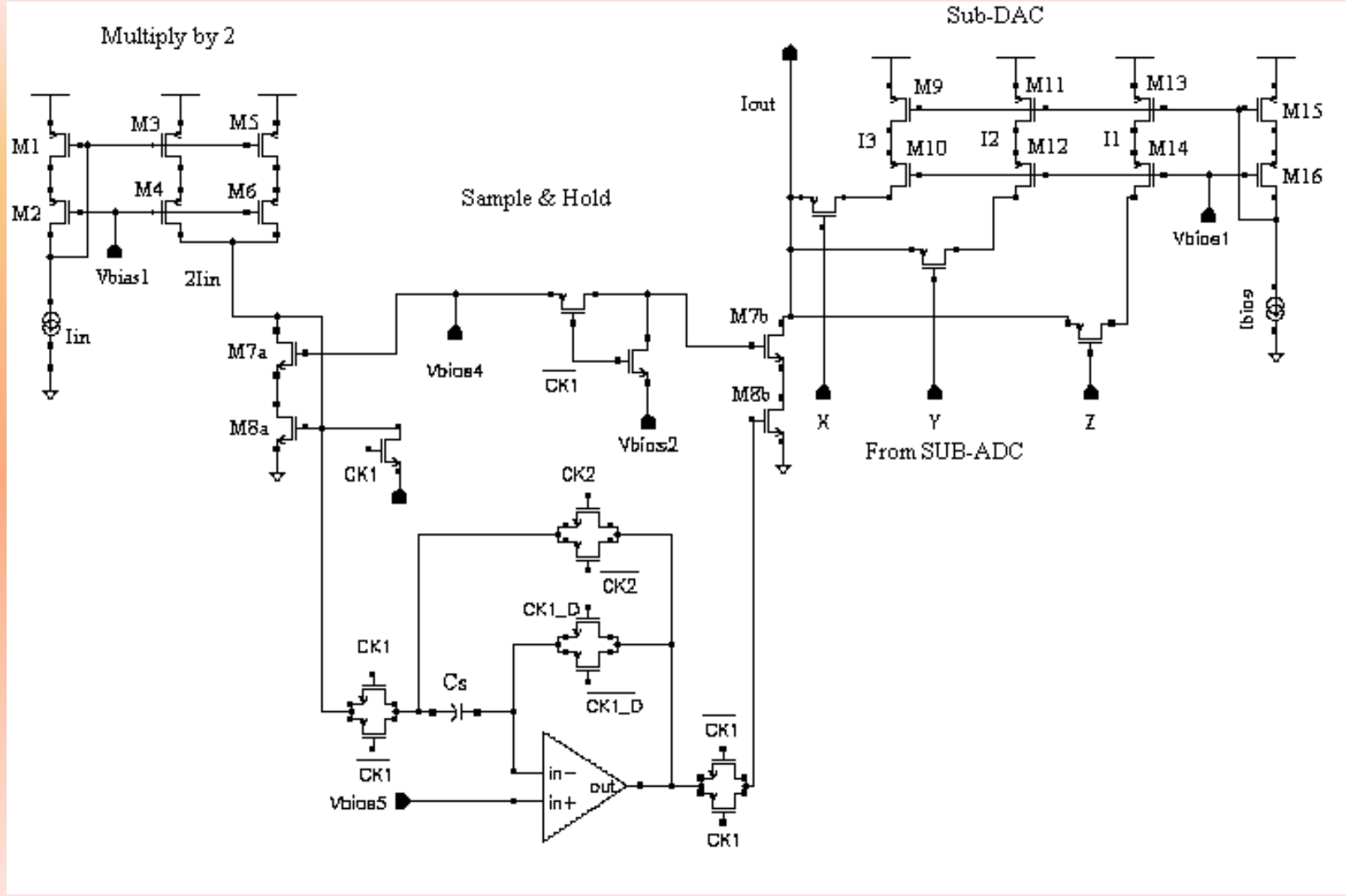


Sub-ADC outputs

$$Iout = \begin{cases} 2I_{in} - I_1 & \text{if} \quad -I_{ref} \le I_{in} < -\dfrac{I_{ref}}{4} \\ 2I_{in} - I_2 & \text{if} \quad -\dfrac{I_{ref}}{4} \le I_{in} < +\dfrac{I_{ref}}{4} \\ 2I_{in} - I_3 & \text{if} \quad +\dfrac{I_{ref}}{4} \le I_{in} \le +I_{ref} \end{cases}$$

00
01
10

Schematic Design of Current Mode MDAC

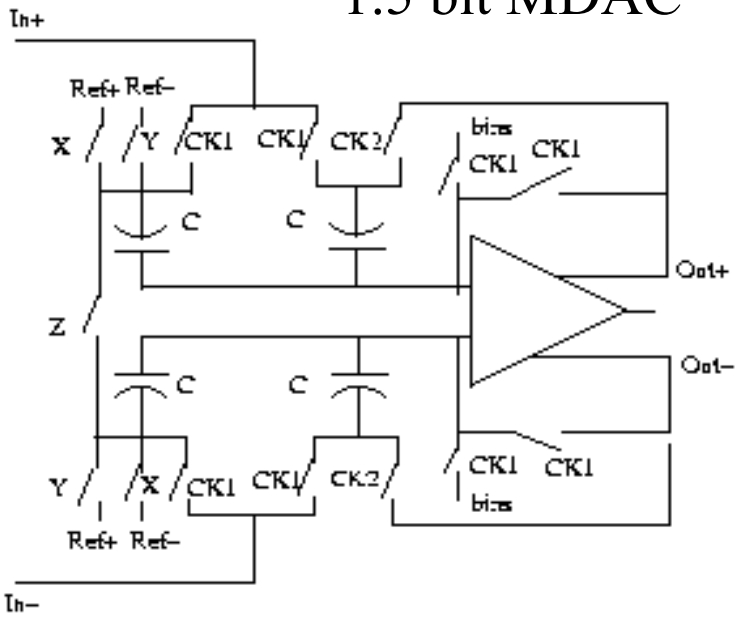


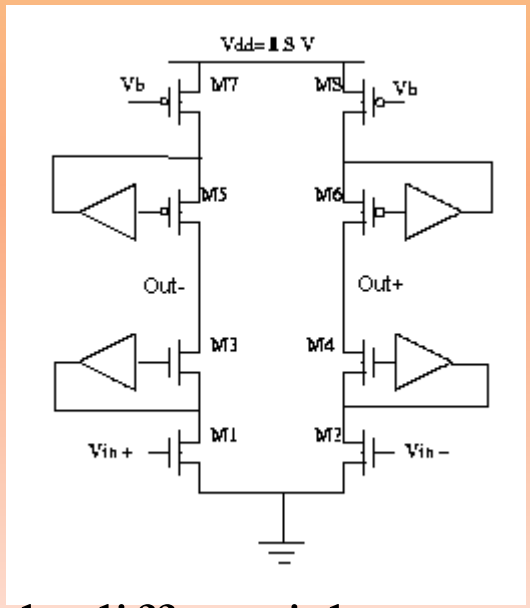
Voltage Mode Stages

$$Vout = \begin{cases} 2V_{in} - V_{ref} & \text{if} \quad -V_{ref} \le V_{in} < -\dfrac{V_{ref}}{4} \\ 2V_{in} & \text{if} \quad -\dfrac{V_{ref}}{4} \le V_{in} < +\dfrac{V_{ref}}{4} \\ 2V_{in} + V_{ref} & \text{if} \quad +\dfrac{V_{ref}}{4} \le V_{in} \le +V_{ref} \end{cases}$$

Sub-ADC outputs
00
01
10

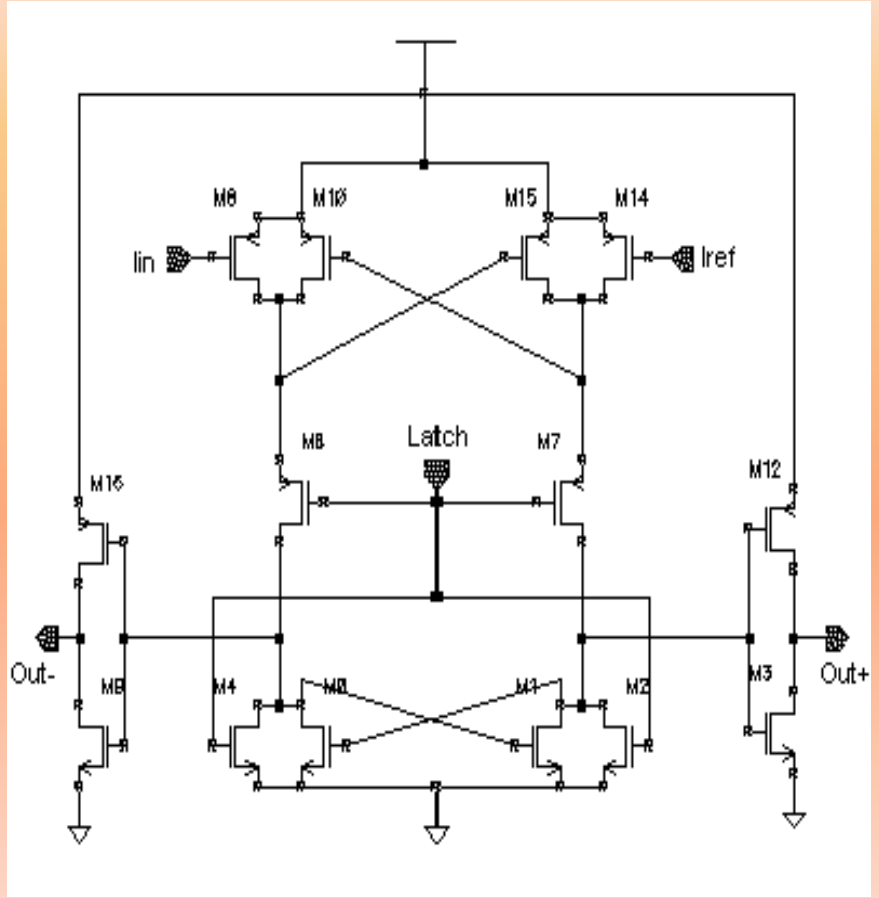
1.5 bit MDAC



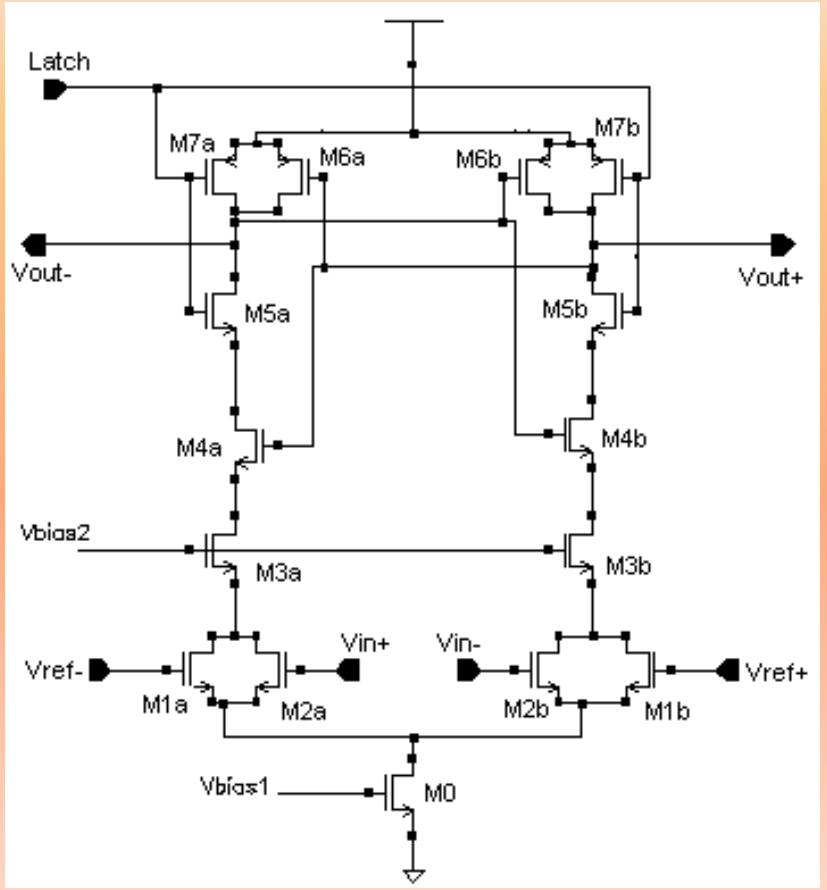


Pseudo-differential op-amp

Zero static power latch comparator

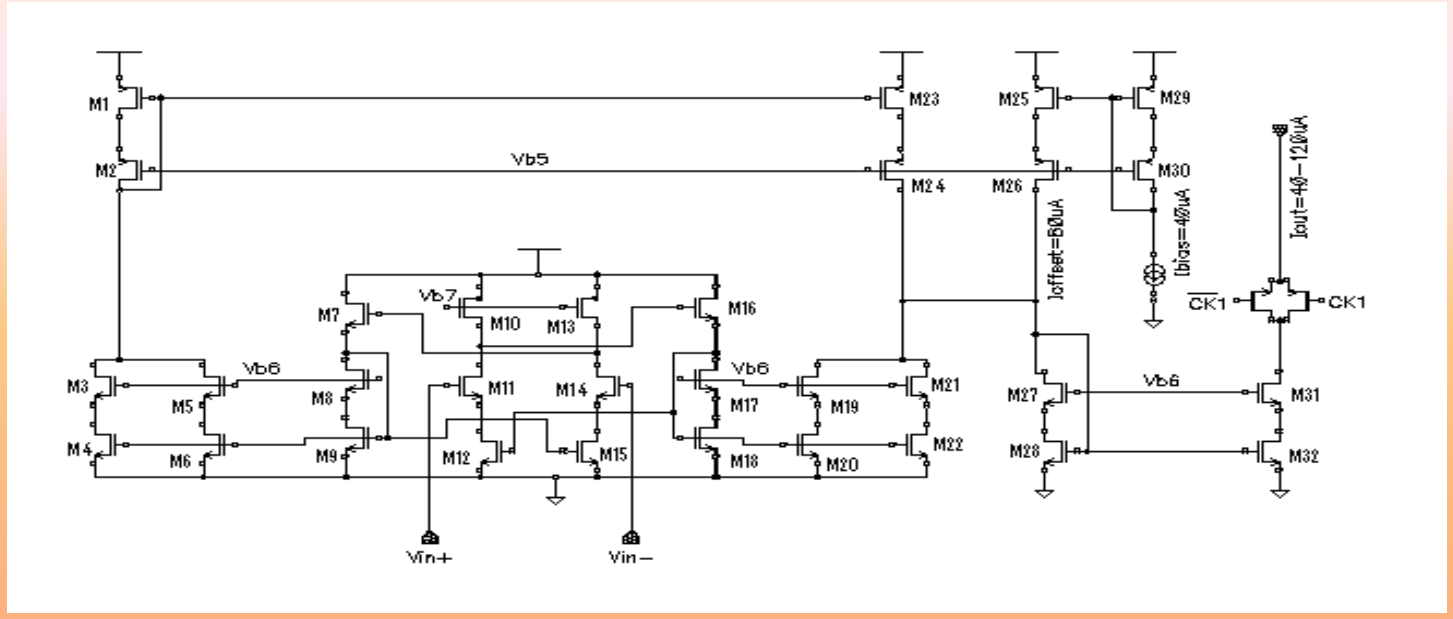


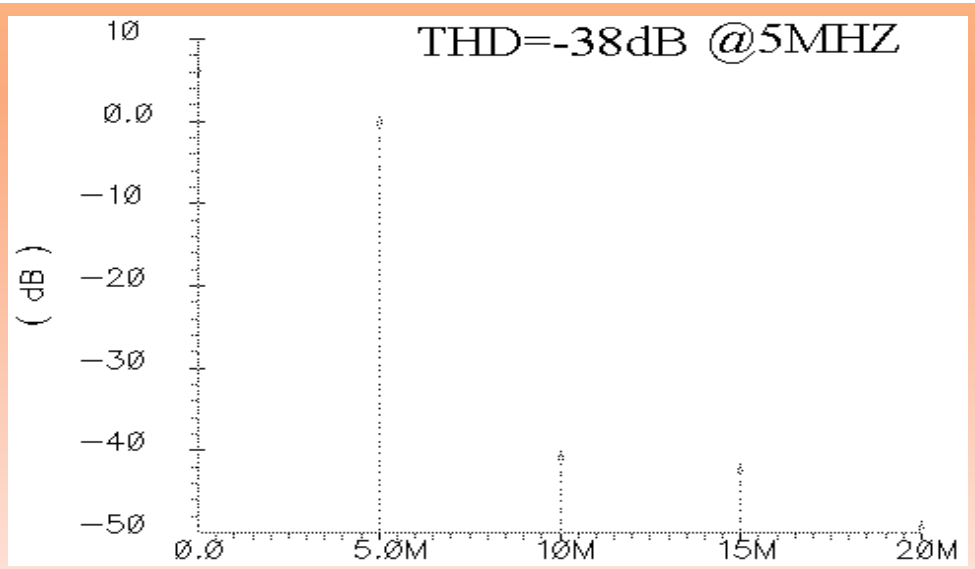
Current comparator



Improved resolution Voltage comparator

Low Power Voltage-to-Current Converter





Estimation of Power dissipation and Area

Proposed Architecture

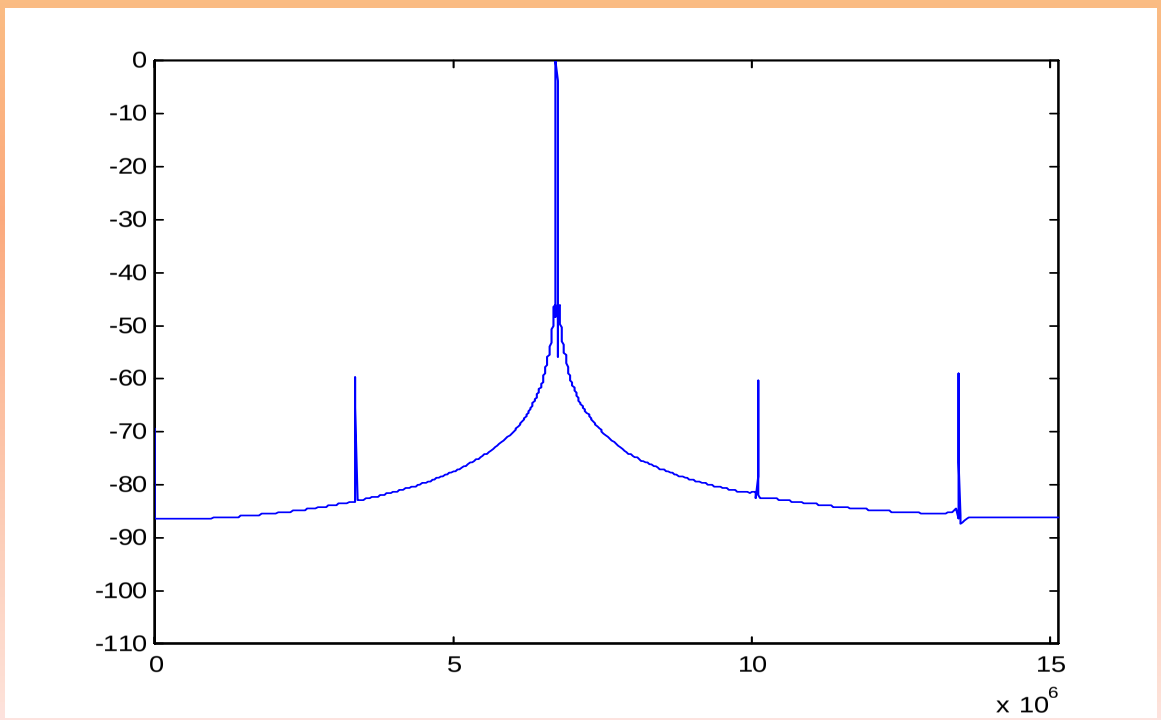
Stage	Type	Sampling capacitor	Power dissipation	Area mm^2
S/H	PD	0.5pF	2.2mW	0.011
1^{st},2^{nd}	PD	0.5pF	2.45mW	0.0284
3^{rd}	D	0.4pF	3.84mW	0.0315
VIC	S		2.4mW	0.012
4-7^{th}	S	0.25pF	1.1mW	0.019
8-10^{th}	S	0.25pF	0.8mW	0.019
11^{th}	S		0.3mW	0.004
Total			20.44mW	0.2483

Fully differential Architecture

Stage	Type	Sampling capacitor	Power dissipation	Area
S/H	PD	0.5pF	4.2mW	0.014
1^{st},2^{nd}	PD	0.5pF	4.5mW	0.032
3-5^{th}	PD	0.4pF	3.84mW	0.0315
6-8^{th}	PD	0.3pF	2.5mW	0.03
9-10^{th}	D	0.2pF	2 mW	0.025
11^{th}			0.3mW	0.0195
Total			36.52mW	0.332

Results

Technology	0.18-μm TSMC CMOS
Supply Voltage	1.8 V
Resolution	12-bits
Sampling Rate	30-Msample/s
Full Scale input range	1.4 V_{P-P}
SFDR@6.73MHZ	59.2 dB
Estimated Area (Including digital circuits)	0.345 mm^2
Estimated Power dissipation	22mW



Conclusion

-Proposed Architecture using combination of pseudo-differential and current mode is suitable for design of low-power, low-area and high-speed ADCs.

-By Improving the Voltage-to-Current converter much better accuracy can be achieved.