Analog CMOS IC Design

Improved Initial Overdrive Sense-Amplifier For Low-Voltage DRAMS

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Introduction

Key Overall Chip Parameters for High-Performance Logic, from 2001 ITRS

		Near Term							Long Term		
Calendar Year		2001	2002	2003	2004	2005	2006	2007	2010	2013	2016
DRAM Half Pitch	nm	130	115	100	90	80	70	65	45	35	22
Physical Gate Length, L_g	nm	65	53	45	37	32	28	25	18	13	9
Nominal Power Supply Voltage (Vdd)	V	1.2	1.1	1.0	1.0	0.9	0.9	0.7	0.6	0.5	0.4
Maximum on-chip local clock frequency	GHz	1.7	2.3	3.1	4.0	5.2	5.6	6.7	11.5	19.4	28.8
Allowable maximum power dissipation, with heatsink	W	130	140	150	160	170	180	190	218	215	288
Number of transistors per chip	Millions of transistors	276	348	439	553	697	878	1106	2212	4424	8848

- The DRAM half pitch and L_g are drivers of IC technology scaling, including lithography
- Technology generations (in red) defined by DRAM half pitch
  - This is a dense feature: drives functional density and Litho. and Etch
  - –Reduction factor of 0.7X ~ $1/\sqrt{2}$ between generations (130nm in 2001, 90nm in 2004, 65nm in 2007, etc.)
  - –Three years between generations
- –Gate length (L_g) $\leq$ 0.5 X DRAM half pitch
  - –These are isolated features
  - –Rapid scaling of L_g is driven by need to improve transistor speed

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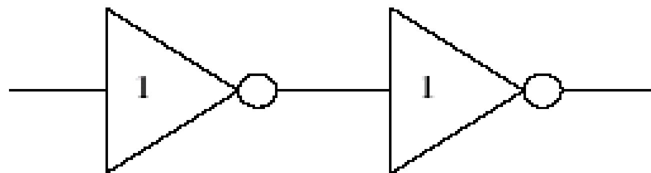
Goals and Objectives

- The goal of this project is to improve an ‘Initial Overdriven Sense Amplifier For Low-Voltage DRAMS’, initially proposed by Jyi-Tsong Ling and Cheng-Chih Hsu, published in 2000 IEEE.
- Removing redundant parts and modifying the existing circuit.
- Lowering the Aspect Ratio (W/L) where needed in order to attain the desired delay.
- A range of supply voltages, 1.3V-2.0V, will be used for testing and results will be compared for the optimum power supply value.
- A range of Boost Capacitance were tested ranging from 50fF – 500fF

Gate Sizing

1 Identical cascaded inverters

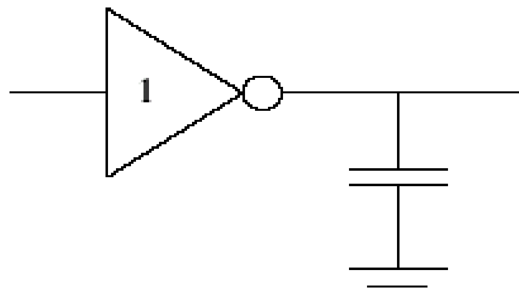


$$t_p = 0.69R_1(C_{dn1} + C_{dp1} + C_{gn2} + C_{gp2})$$
$$= 0.69R(C_d + C_g) = 0.69RC_d(1 + \frac{C_g}{C_d}) = t_{p0}(1 + \frac{1}{\gamma})$$

where

$$t_{p0} = 0.69RC_d \qquad \gamma = \frac{C_d}{C_g} \qquad C_d = \gamma C_g$$

2 Loaded inverter



$$t_p = 0.69R(C_d + C_L) = t_{p0}(1 + \frac{C_L}{C_d}) = t_{p0}(1 + \frac{C_L}{\gamma C_g})$$

Introduction

DRAM Functionality and The Sense Amplifier

DRAM Introduction

- **DRAM:** Dynamic Random Access Memory
- ***Single Transistor*** to store one bit.
    - Reading the bit can disturb the information.
    - To prevent loss of information, periodic ***refreshment*** of the transistors are required.
    - All the bits in a row are refreshed simultaneously.
    - Every DRAM cell must access every row within certain time window. Typically about 8 msec.
    - The speed of a DRAM is mostly dependent on the READ and WRITE time, which are affected by the Sense Amplifier.

1-Bit DRAM Memory Cell

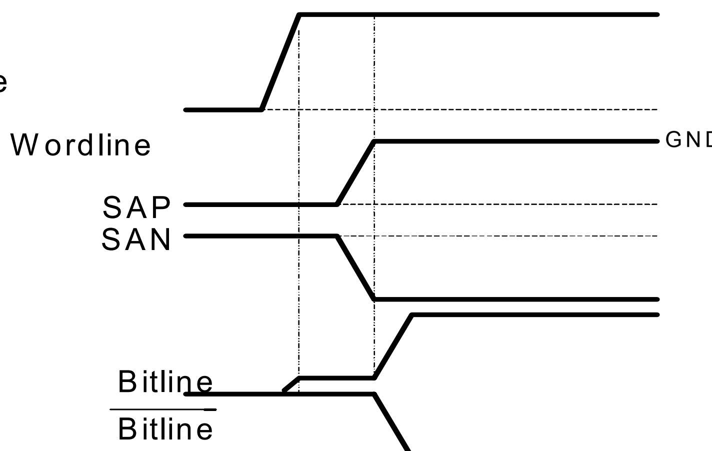


Fig 1. 1-Bit DRAM Structure

Originally Proposed Sense Amplifier

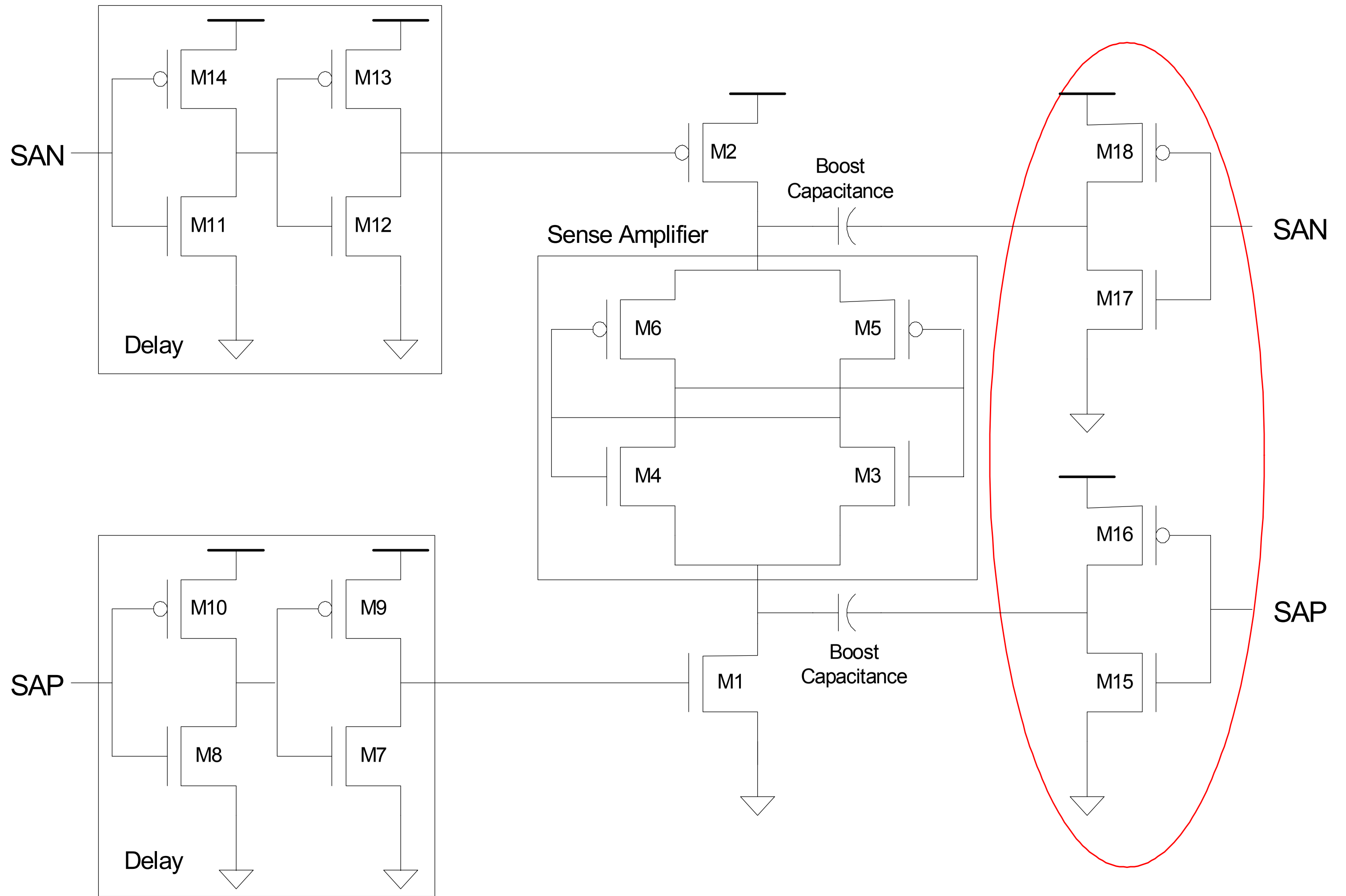


Fig 2. Original Sense Amplifier

Sense Amplifier Gate Sizes

Original Sense Amplifier		
Transistor	Width (nm)	Length (nm)
M1	500	180
M2	1200	180
M3	500	180
M4	500	180
M5	1200	180
M6	1200	180
M7	220	225
M8	220	300
M9	220	4500
M10	220	4500
M11	220	4500
M12	220	4500
M13	220	350
M14	220	225
M15	220	225
M16	220	1200
M17	220	225
M18	220	225

Table 1. Original Transistor Size

Improved Sense Amplifier		
Transistor	Width (nm)	Length (nm)
M1	500	180
M2	1200	180
M3	500	180
M4	500	180
M5	1200	180
M6	1200	180
M7	3000	220
M8	5000	180
M9	220	225
M10	220	5000
M11	220	4000
M12	220	225
M13	220	225
M14	5000	180

Table 2. Improved Transistor Size

Improved Sense-Amplifier

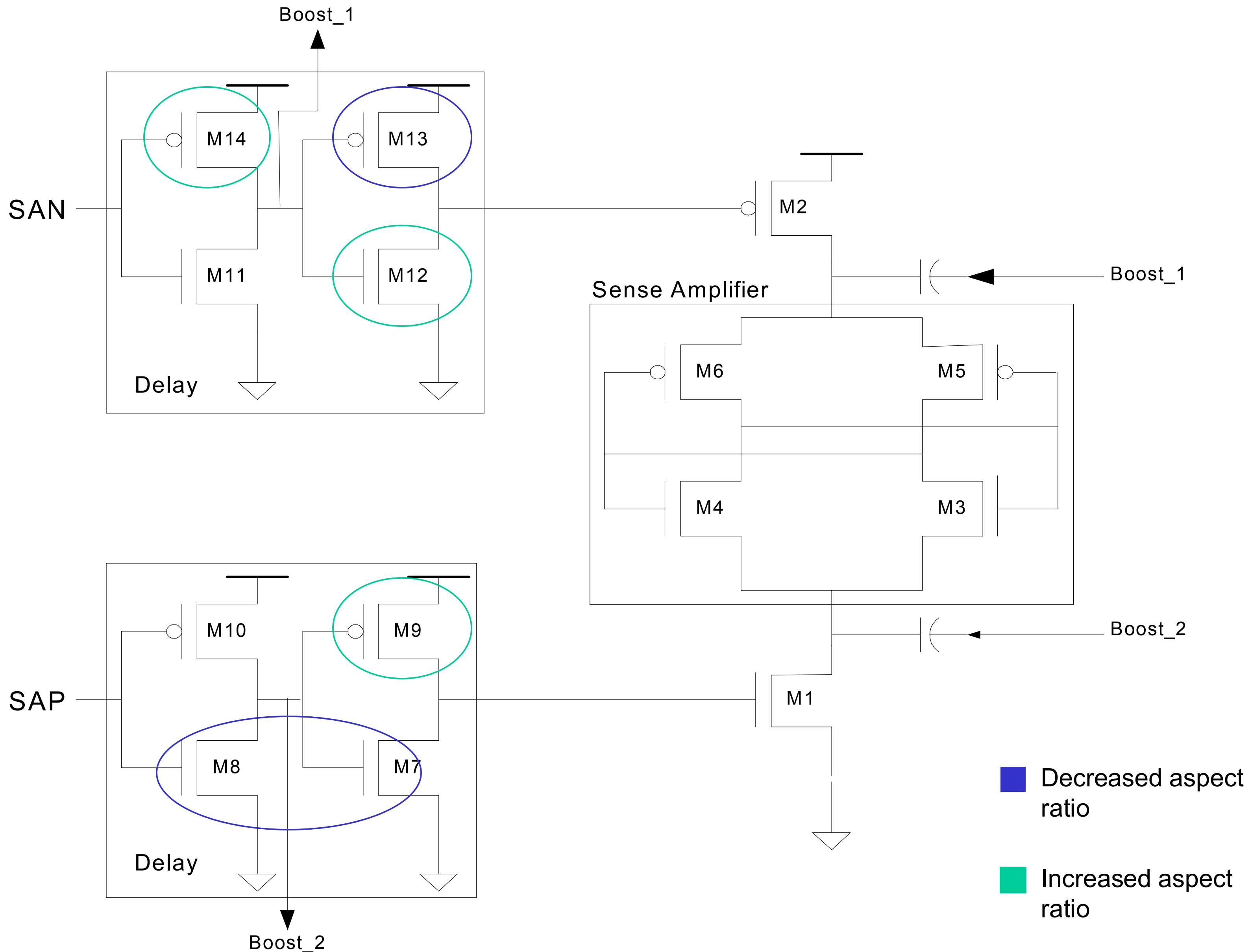


Fig 3. Improved Sense Amplifier

Sense Time Vs VDD

- The most optimum voltage level was found to be 1.5V
- Sensing time improves for voltages less than 1.55V and greater than 1.7V

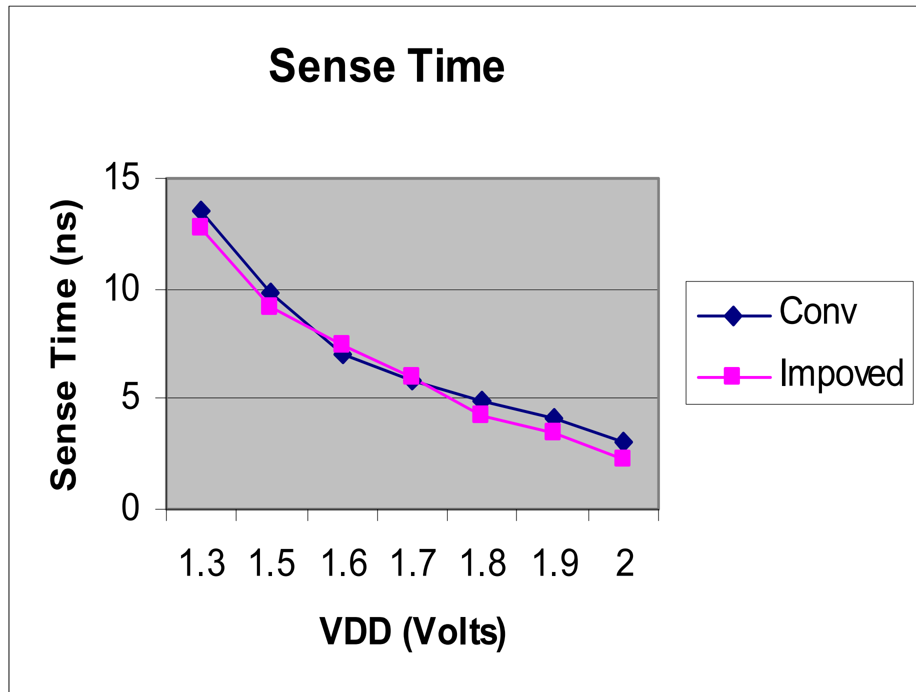


Fig 4. Sense Time

Sense Time (Improved)	
Power (uW)	VDD (V)
12.7	1.3
9.1	1.5
7.4	1.6
6	1.7
4.3	1.8
3.4	1.9
2.3	2

Table 3. Improved Sense Time

Sense Time	
Power (uW)	VDD (V)
13.6	1.3
9.8	1.5
7.1	1.6
5.9	1.7
4.9	1.8
4.1	1.9
3.1	2

Table 4. Original Sense Time

Sense Amplifier Power Consumption

- The lower the voltage the better the power consumption of the Improved Sense Amplifier

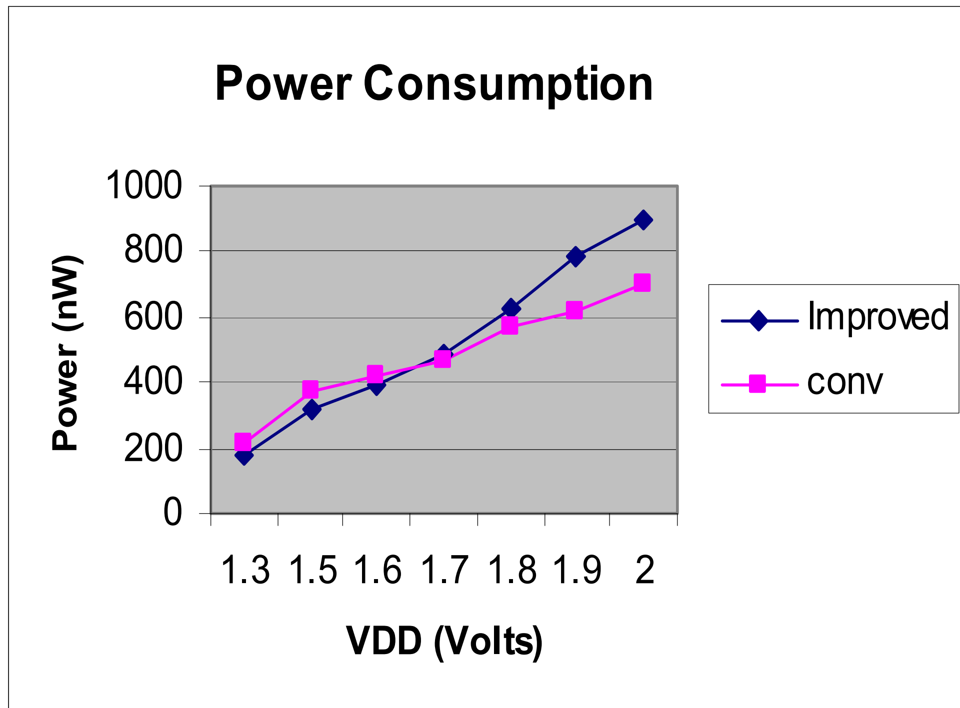


Fig 4. Power Consumption

Power Consumption	
Power (nW)	VDD (V)
219	1.3
375	1.5
424	1.6
471	1.7
567	1.8
620	1.9
700	2

Table 5. Original Power

Power Proposed	
Power (nW)	VDD (V)
177.9	1.3
314.3	1.5
392.8	1.6
489.6	1.7
627.7	1.8
782.9	1.9
897.2	2

Table 6. Improved Power

Sensing Logic High

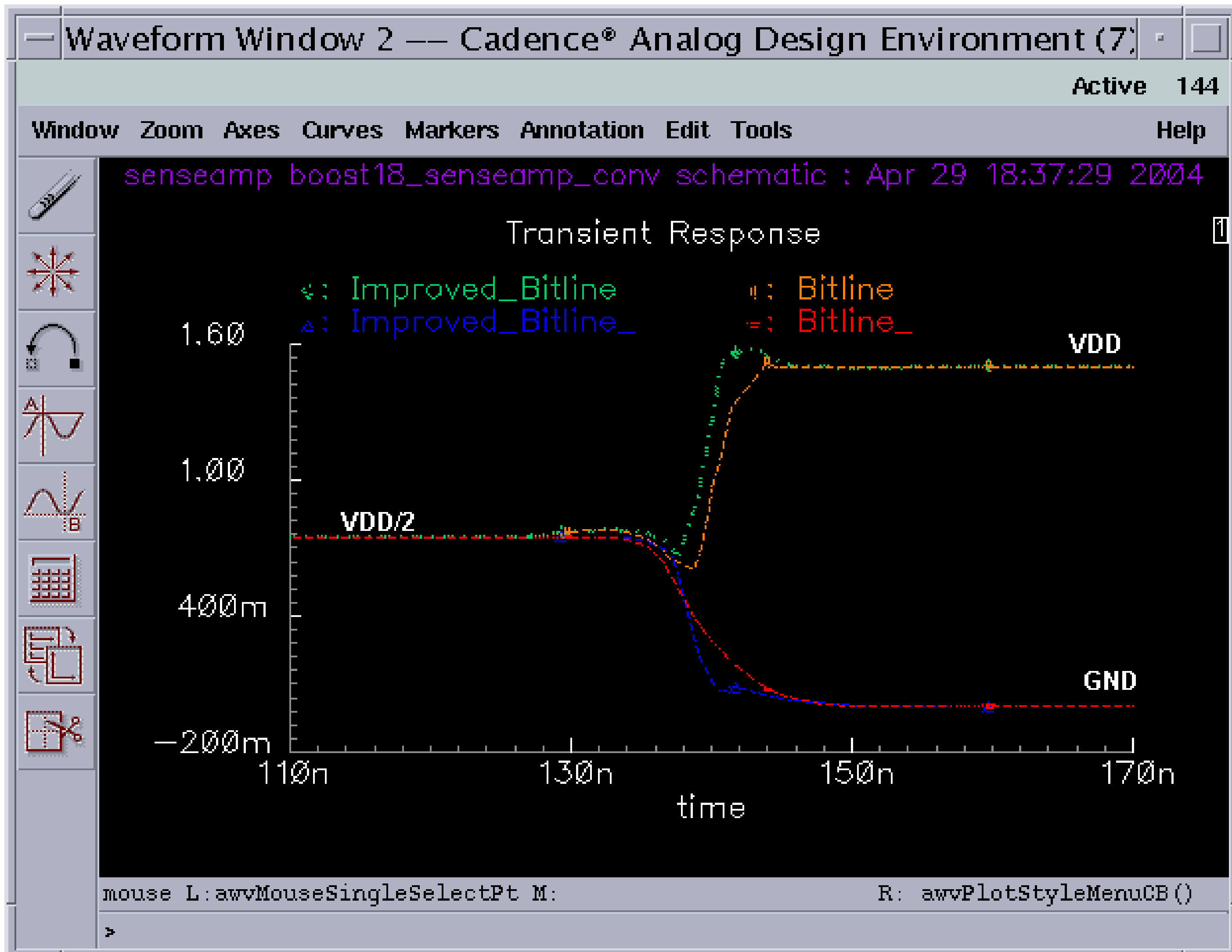


Fig 5. Sense Time Comparison for logic high

Sensing Logic Low

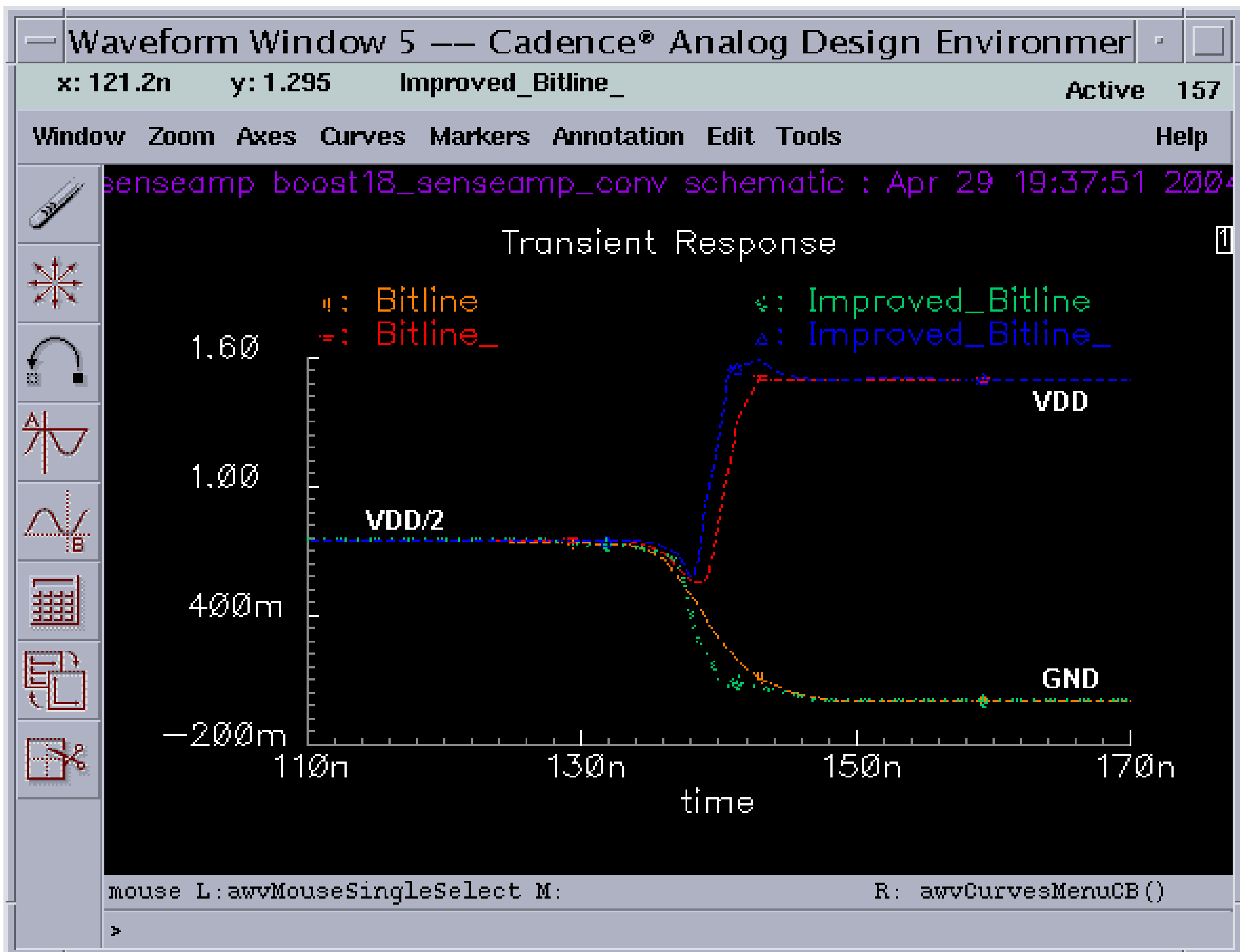


Fig 6. Sense Time Comparison for Logic Low

AC Response

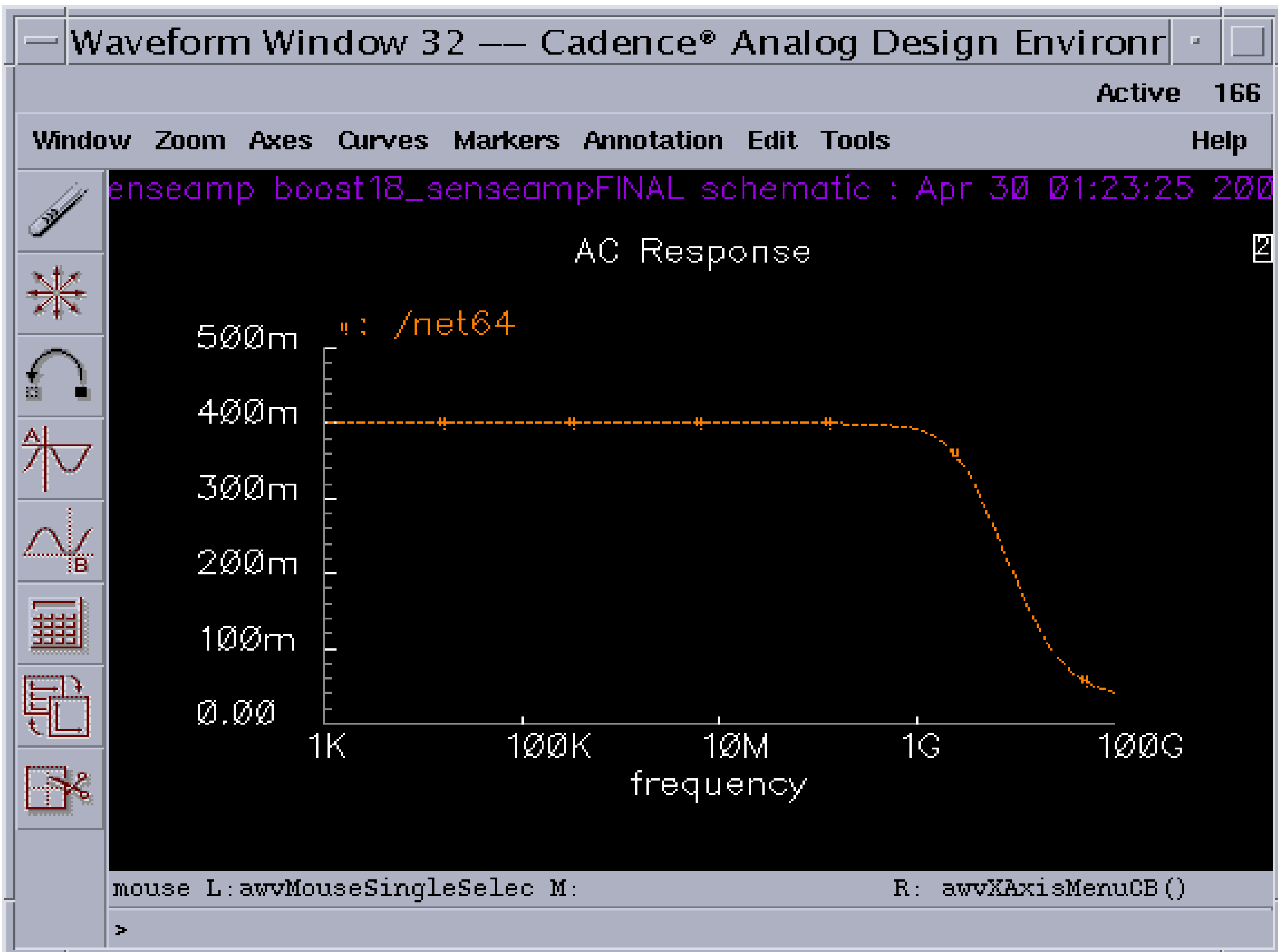


Fig 7. Sense Time Comparison for Logic Low

Observation

- The number of transistors were reduced from 18 to 14.
- Amplifier sense time was reduced by 7.14% compared to the initially proposed.
- The power consumption of the circuit was improved by about 16.2%.
- Sense voltage range was not improved as desired.
- Also, the sense amplifier didn’t perform as well as expected for a Boost Capacitance greater than 100fF.
- Further, a more pronounced improvement can be obtained with more time.

References

[1] Jyi-Tsong Lin et al, “An Initial Overdriven Sense Amplifier For Low Voltage DRAMS”, IEEE 2000

[2] Duane G. Laurent, “Sense Amplifier Signal Margins and Process Sensitivities” Vol. 49, No. 3, March 2002 IEEE

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