Low Power CMOS Analog Multipliers

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1. Application of Analog Multipliers

Analog multiplier is an important subcircuit for many applications such as adaptive filters, frequency doublers, and modulators. It performs linear product of two continuous signals x and y, yielding an output $z = Kxy$, where K is a constant with suitable dimension[1].

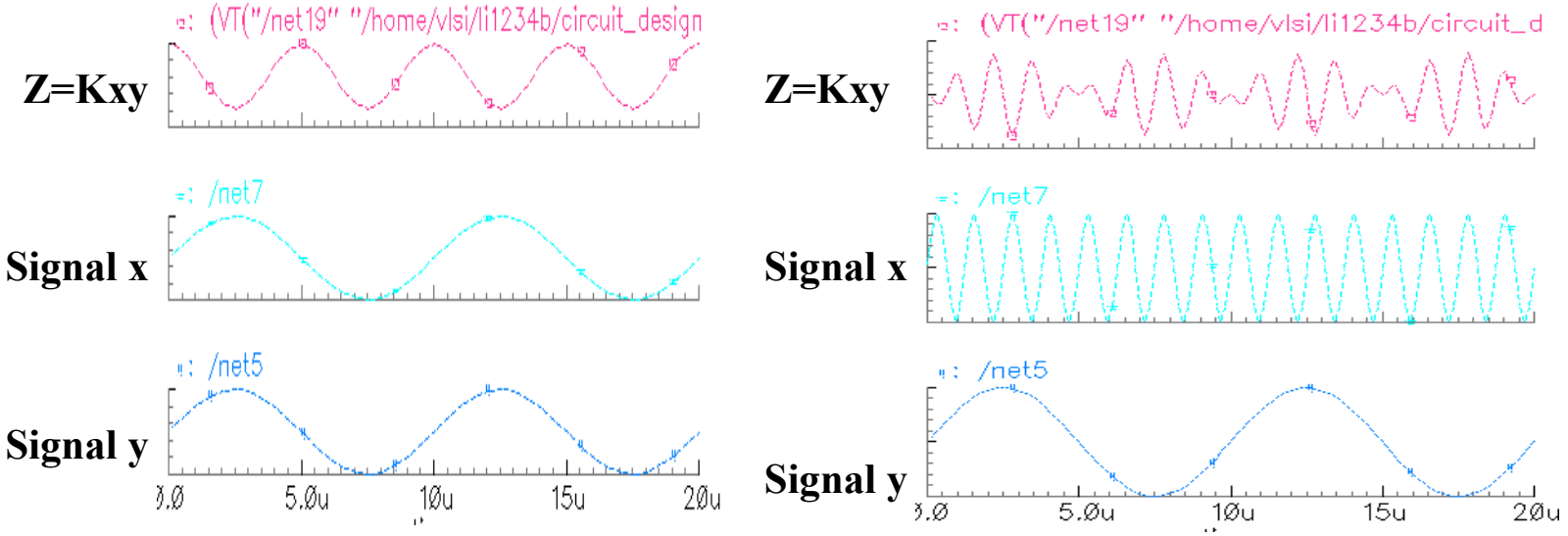


Fig 1 The Application of Analog Multiplier

2. Performance Metrics of Analog Multipliers

The linearity, supply voltage, power dissipation and noise are the main metrics of performance [3]. We try to design some specific structures or topologies for the analog multiplier that have low power dissipation while at the same time keeping good linearity, low supply voltage and low noise.

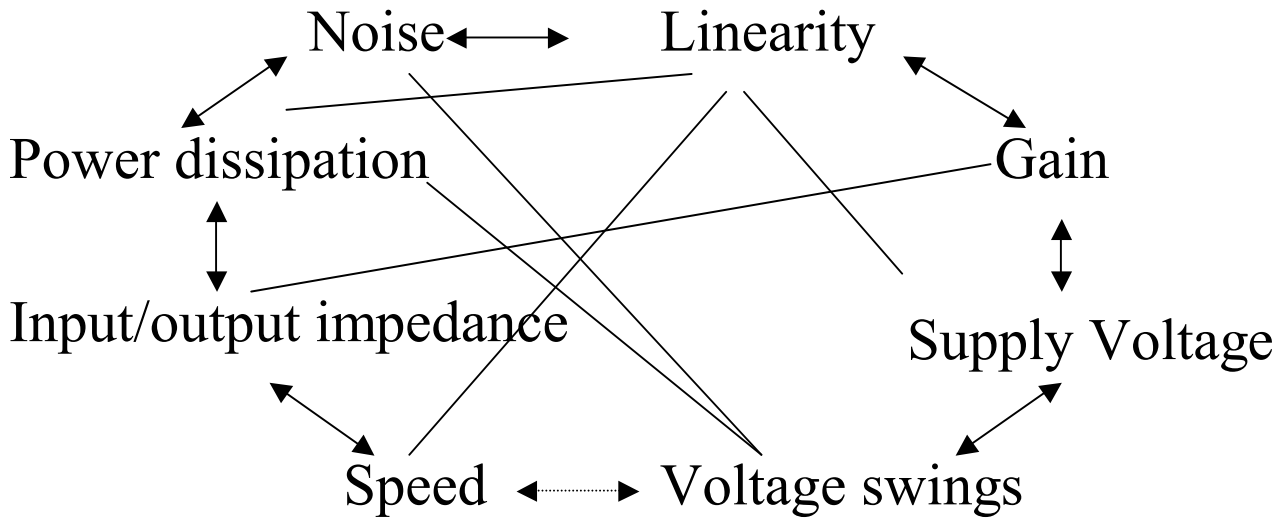


Fig 2 The Metrics of Analog Multiplier

3. Basic Idea of Our Low Power Design

Use total current to represents the power consumption

$$I_D = \frac{1}{2}K(V_{GS} - V_{TH})^2(1 + \lambda V_{DS})$$

$$I_D = K[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2]$$

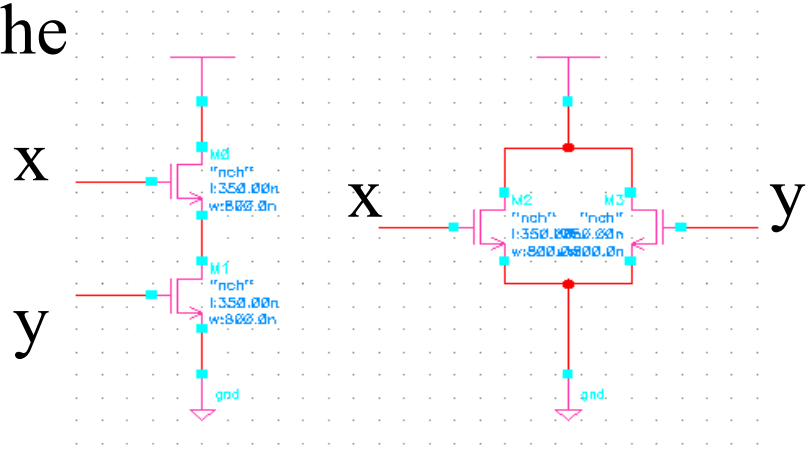
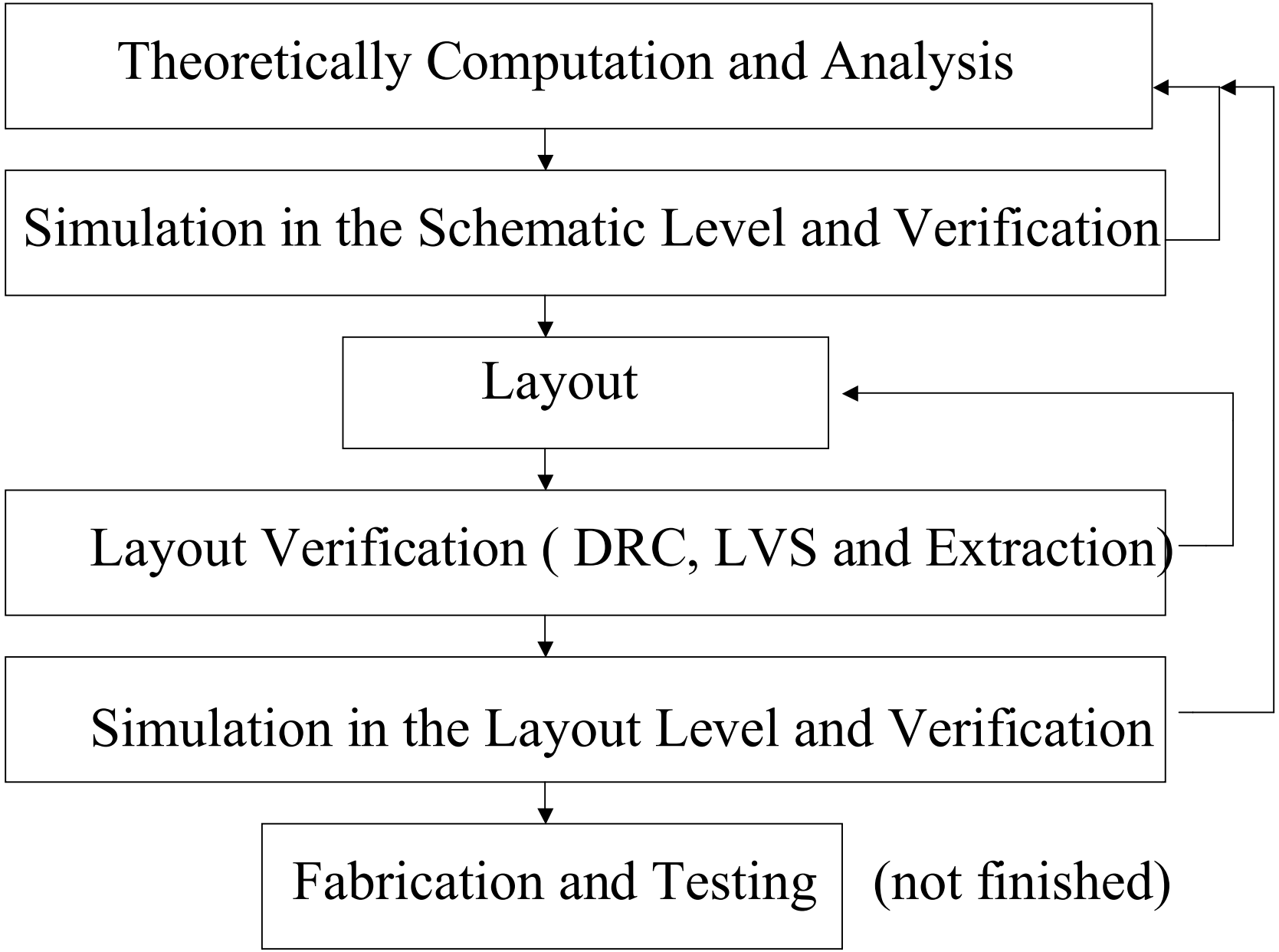


Fig. 3. Power consumption and input range for (a) series structure and (b) parallel structure

[3]Where $K = \mu_o C_{ox} W/L$ and V_{TH} are the transconductance parameter and the threshold voltage of the device, respectively, and λ represents the channel-length modulation effect for long channel devices.

By biasing the transistors to operate in the triode region, one can reduce the drain current while keeping a relatively large input range.

4. Design Flow of Our structures



5. Our First Multiplier structure

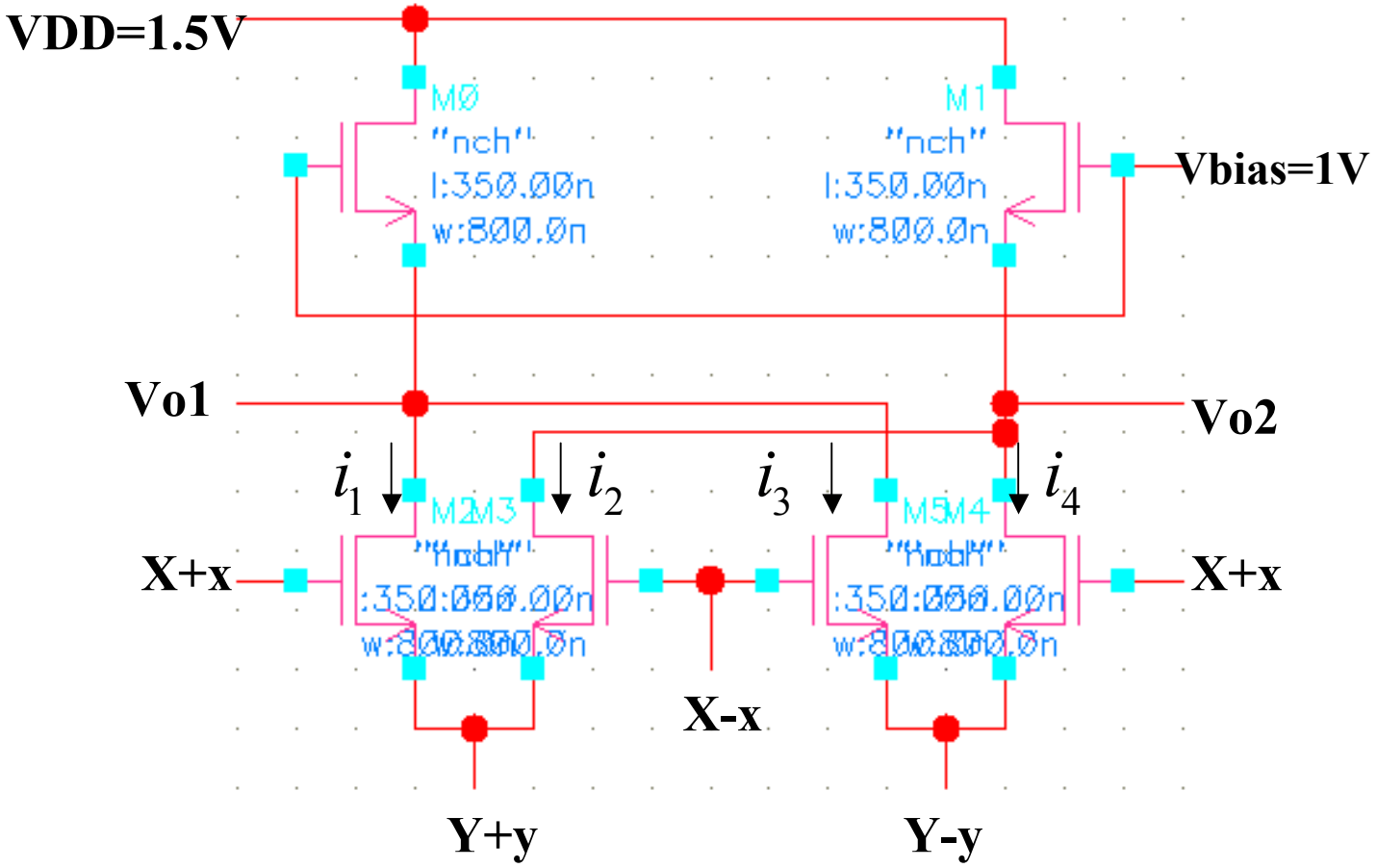


Fig. 4. First Multiplier Structure

6. Theoretical Analysis of First structure

For the transistors working in the triode region, we have the equation for small signal model as $i_d = Kv_{gs}v_{DS}$, therefore, we have:

$$i_1 = Kv_{DS1}(x-y) \qquad v_{DS1} = v_{o1} - Y - y$$

$$i_2 = Kv_{DS2}(-x-y) \qquad v_{DS2} = v_{o2} - Y - y$$

$$i_3 = Kv_{DS3}(x+y) \qquad v_{DS3} = v_{o1} - Y + y$$

$$i_4 = Kv_{DS4}(-x+y) \qquad v_{DS4} = v_{o2} - Y + y$$

By this equations, we have $(i_1+i_3)-(i_2+i_4) = 4Kxy$

The bias conditions is $v_o \le X \pm x - V_{TH}$

$$0 \le Y \pm y < X \pm x - V_{TH}$$

7. Linearity Analysis of First structure

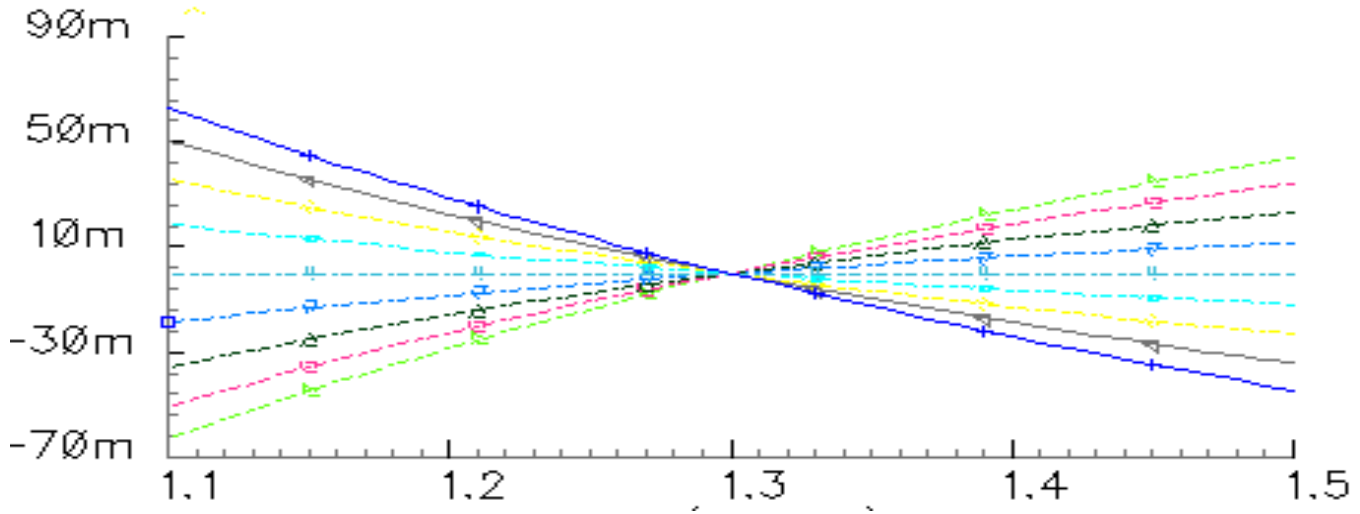


Fig. 5.(a) DC Response for signal x (with body effect)

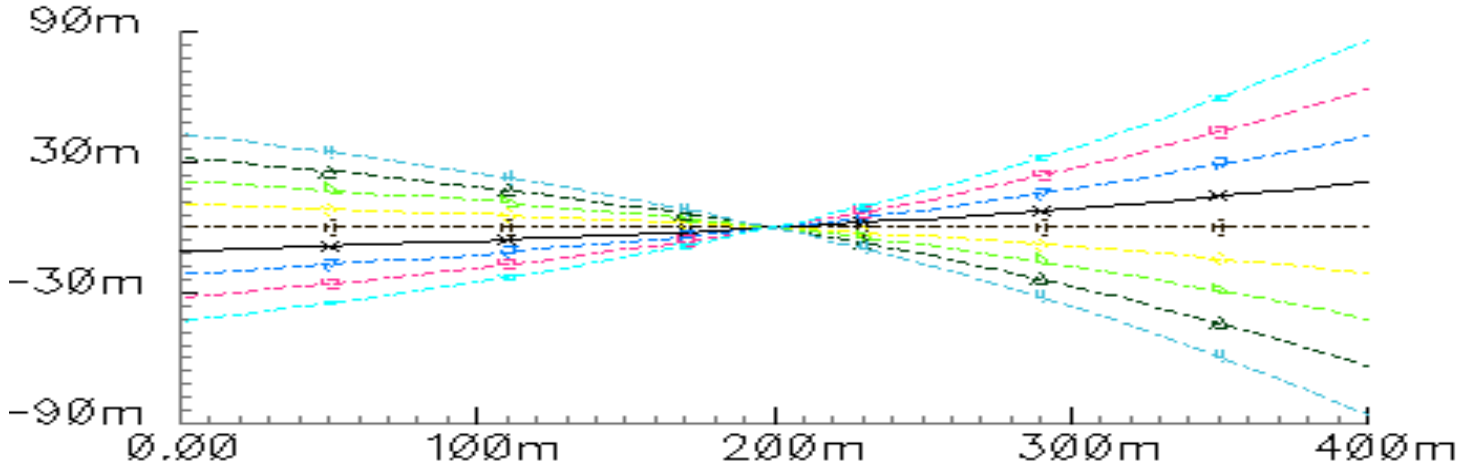


Fig. 5.(b) DC Response for signal y (with body effect)

7. Linearity Analysis of First structure

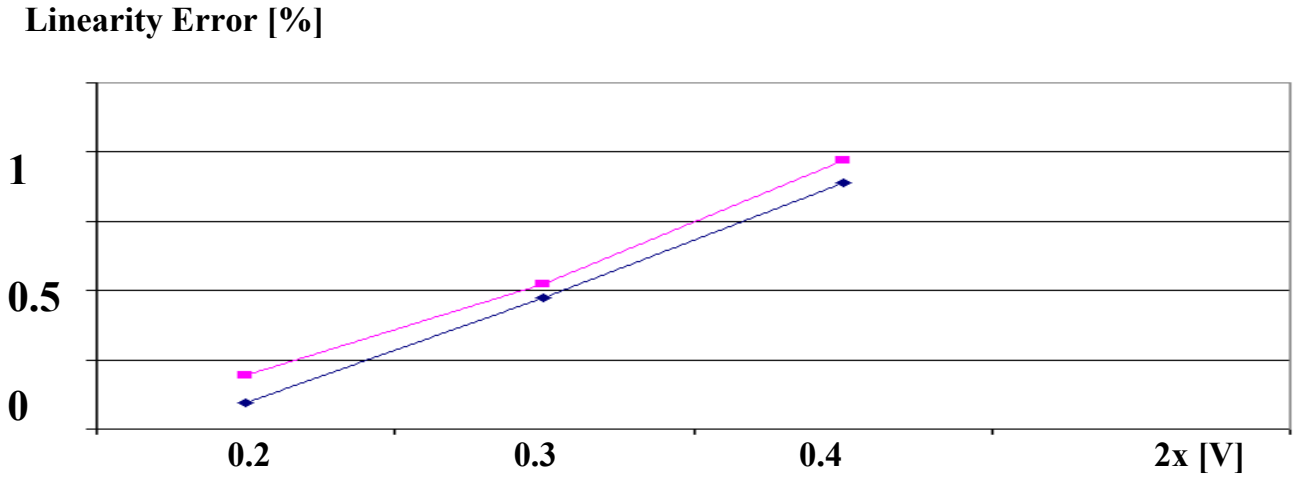


Fig. 6.(a) Linearity Error of signal x with 2y=0.4V (with and without body effect)

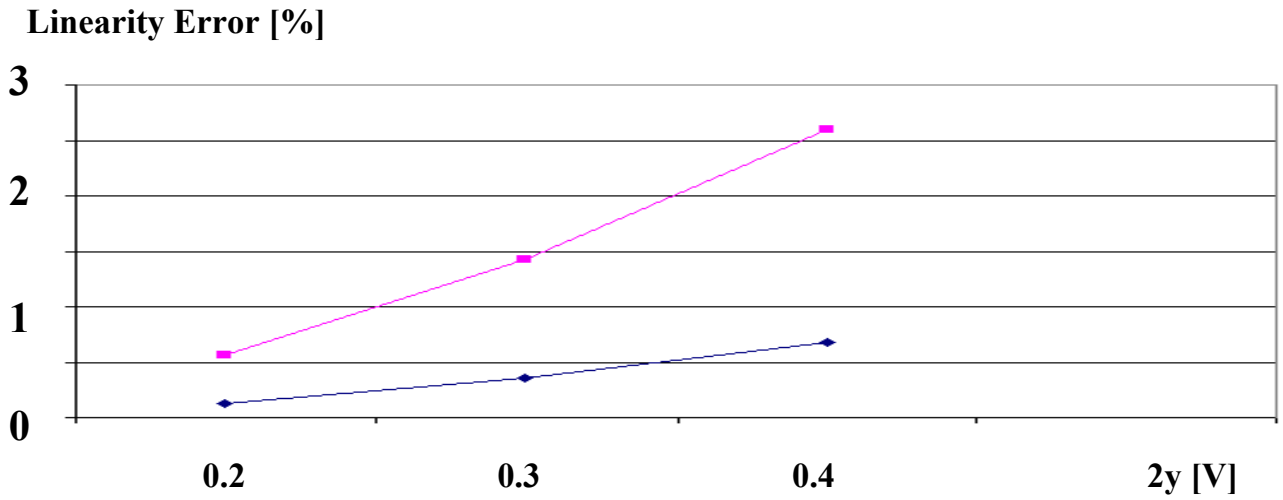


Fig. 6.(b) Linearity Error of signal y with 2x=0.4V (with and without body effect)

8. Power Consumption of First Structure

Power consumption can be estimated by the total supply current if the supply voltage is constant. Because we have

$$I_{total} = i_1 + i_2 + i_3 + i_4$$

$$i_1 + i_3 = 2K_l(X - Y - V_{TH})(V_{o1} - Y) + 2K_l(x + y)y = \frac{1}{2}K_u(V_b - V_{o1} - V_{TH})^2$$

$$i_2 + i_4 = 2K_l(X - Y - V_{TH})(V_{o2} - Y) + 2K_l(-x + y)y = \frac{1}{2}K_u(V_b - V_{o2} - V_{TH})^2$$

Therefore $I_{total} = 2K_l(X - Y - V_{TH})(V_{o1} + V_{o2} - 2Y) + 4K_l y^2$

We could decrease the power consumption by decreasing the (X-Y), K_l and signal y.

8. Power Consumption of First Structure

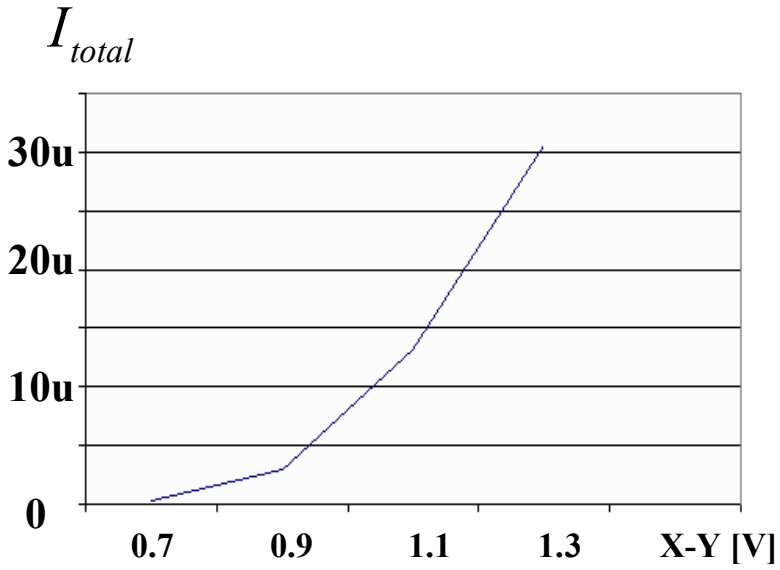


Fig. 7.(a) Total Current Versus X-Y

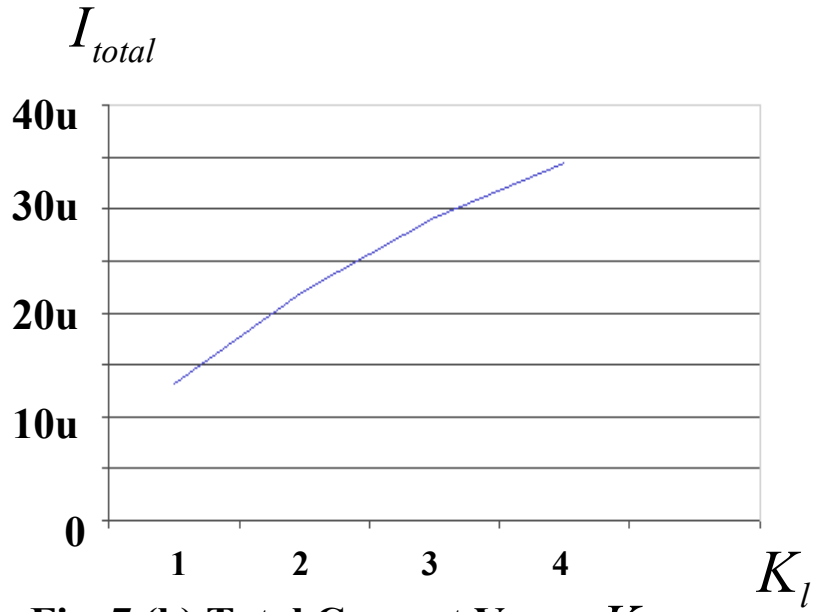


Fig. 7.(b) Total Current Versus K_l

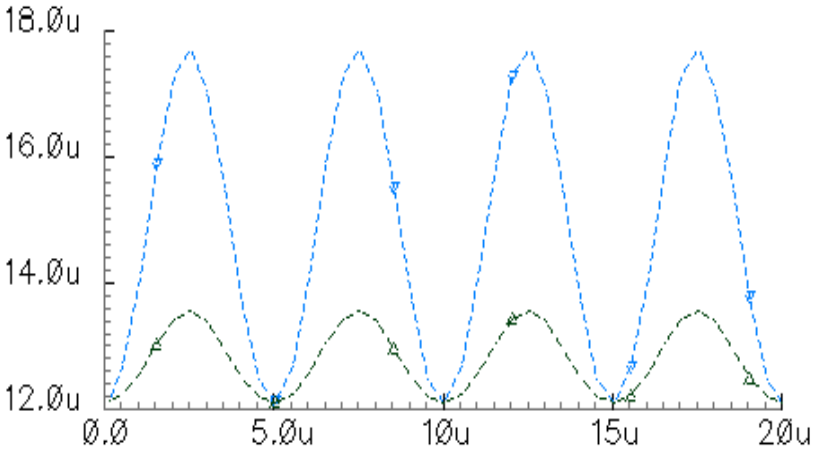


Fig. 7.(c) Total Currents for different signal distribution

9. Noise Analysis of First Structure

The total output noise of Fig. 5 is given by[4]

$$\overline{i_{n;o}^2} = 4\overline{i_{n;lin}^2} + 2\overline{i_{n;sat}^2} = 16KT(g_{ds.l} + \frac{1}{3}g_{m,u})df$$ where

$$g_{ds.l} = K_l(X - V_o - V_{TH})$$ and $$g_{m,u} = 2\sqrt{K_l K_u (X - Y - V_{TH})(V_o - Y)}$$

[2] Hence the input noise is

$$\overline{v_{n;i}^2} \propto \frac{\overline{i_{n;o}^2}}{16K_l^2} = \frac{kT}{K_l}[(X - V_o - V_{TH}) + \frac{2}{3}\sqrt{\frac{K_u}{K_l}}(X - Y - V_{TH})(V_o - Y)]$$

That implies that K_u/K_1 and (X-Y) should be decreased to improve the noise performance.

9. Noise Analysis of First Structure

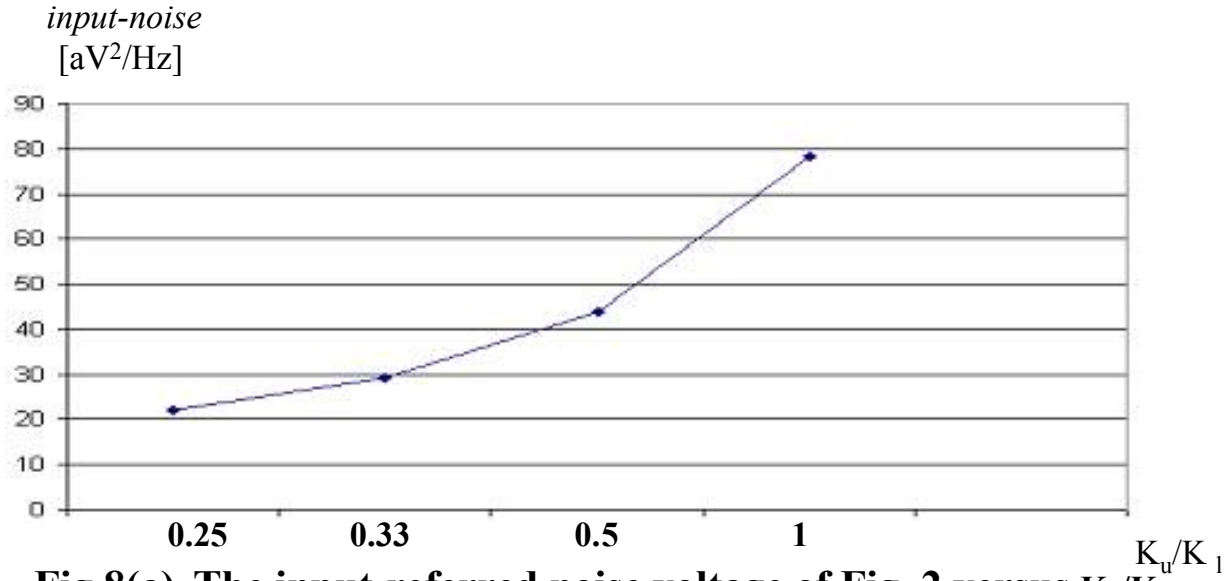


Fig 8(a) The input-referred noise voltage of Fig. 2 versus K_u/K_l

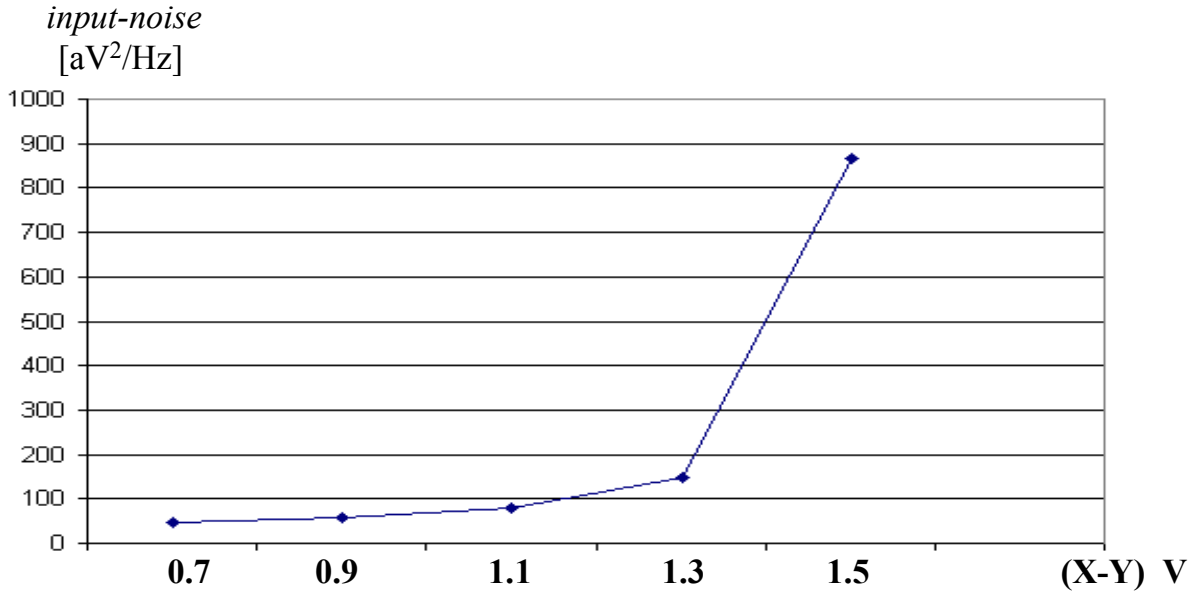


Fig 8(b) The input-referred noise voltage of Fig. 2 versus X-Y

10. Layout of First Multiplier structure

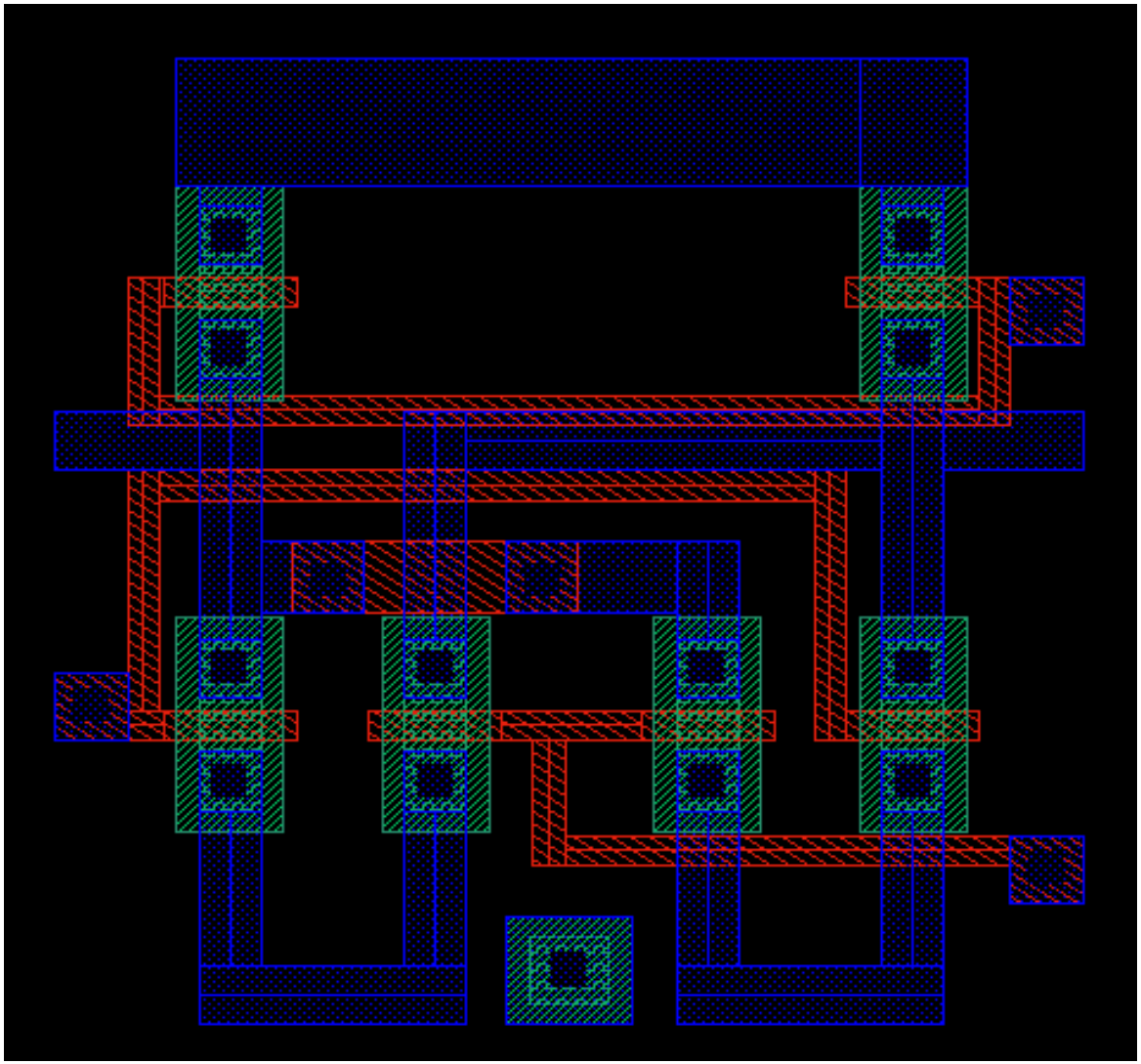


Fig. 9 Layout of our first multiplier structure

10. Layout of First Multiplier structure

When we do the layout of the structures, we consider to:

- Decrease the distance among the transistors as long as we could pass the DRC.
- Try to decrease the length of the metal or polysilicon to decrease the parasite resistors and capacitors involved.
- For the differential structure, try to make involved parasite resistors and capacitors symmetric.

11. Extracted Structure

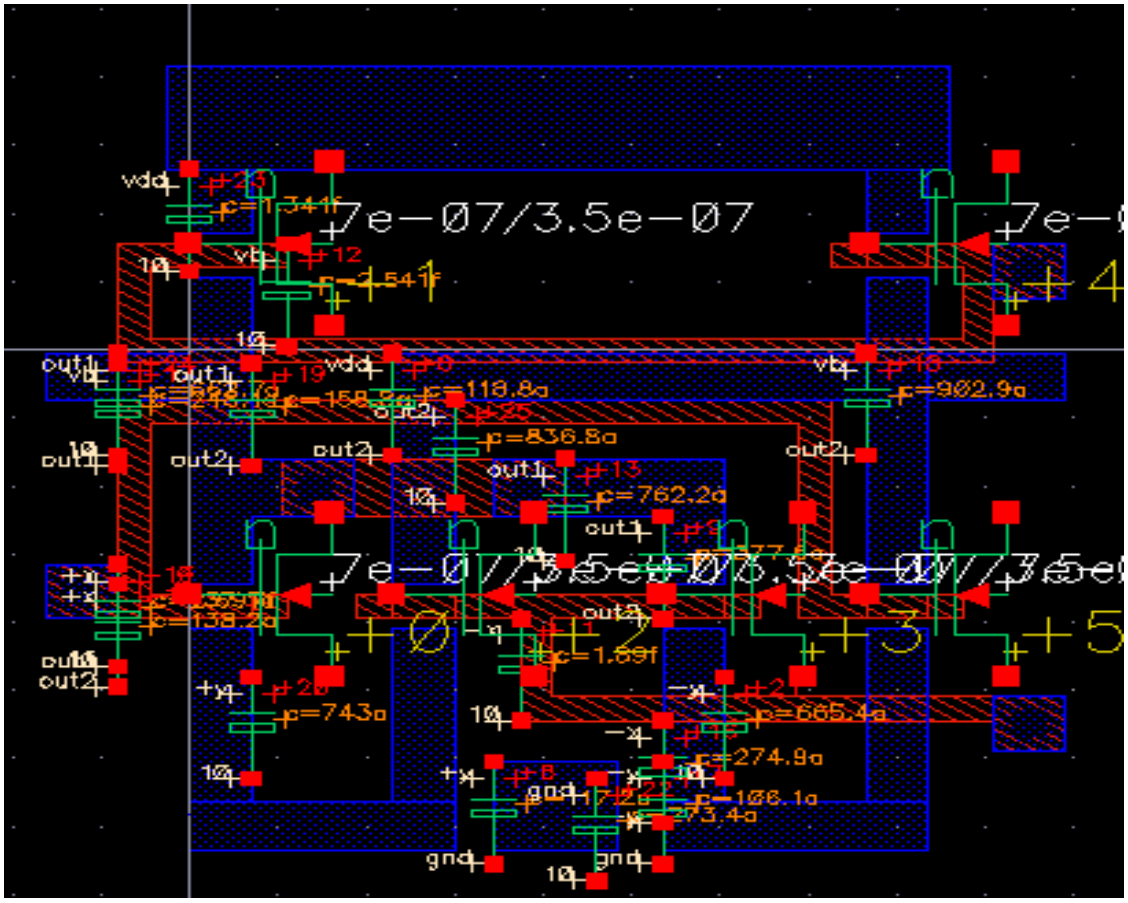


Fig. 10 Extracted First Multiplier Structure

12. Comparison before and after layout

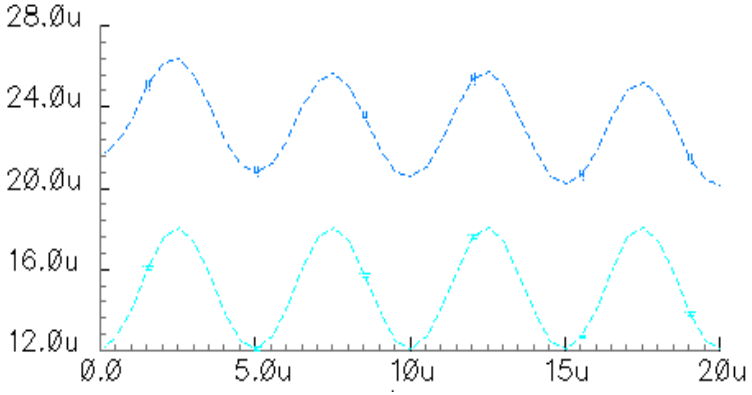


Fig. 11 (a) The comparison of total current before and after layout

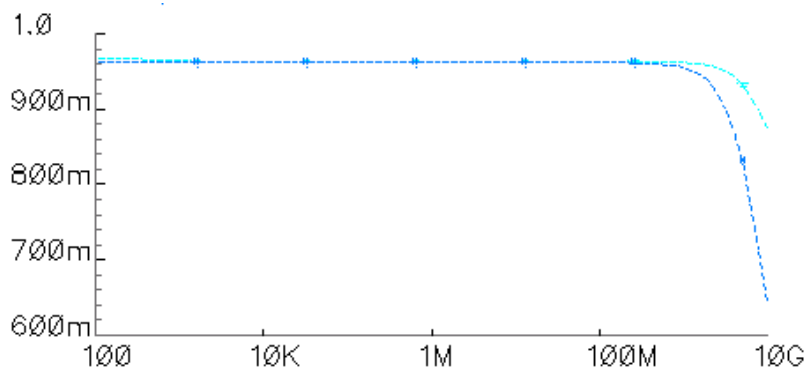


Fig. 11 (b) The comparison of AC response before and after layout

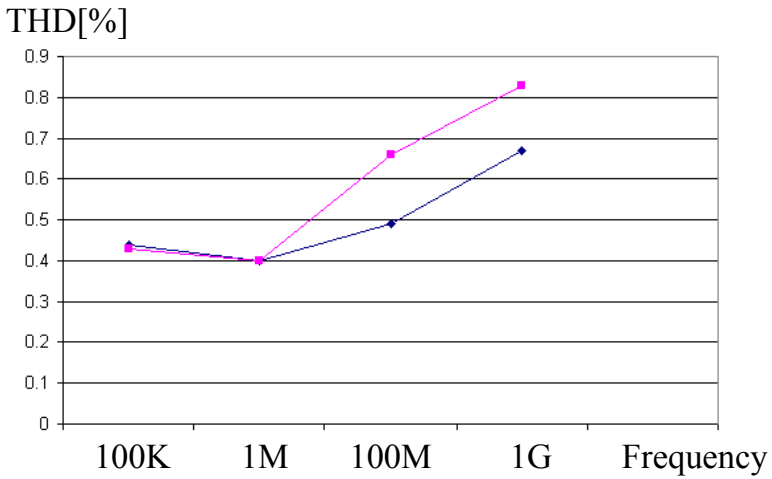


Fig. 11 (c) The comparison of THD for signal 2x=0.4V before and after layout with frequency

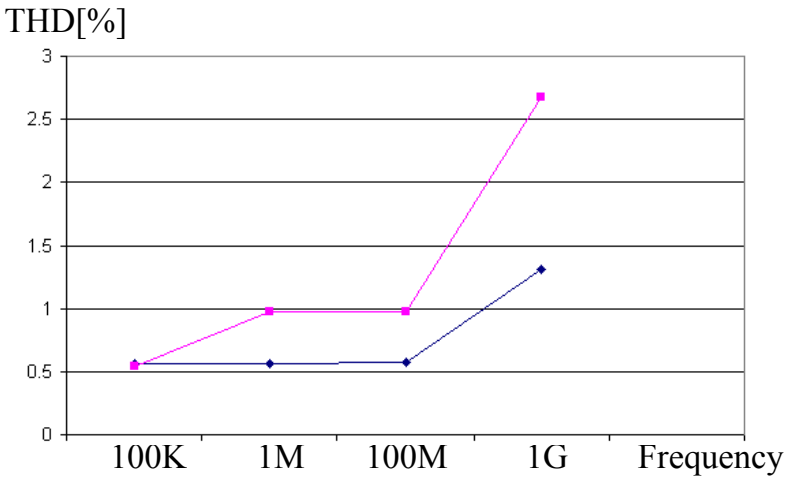


Fig. 11 (d) The comparison of THD for signal 2y=0.4V before and after layout with frequency

13. Our Second Multiplier structure

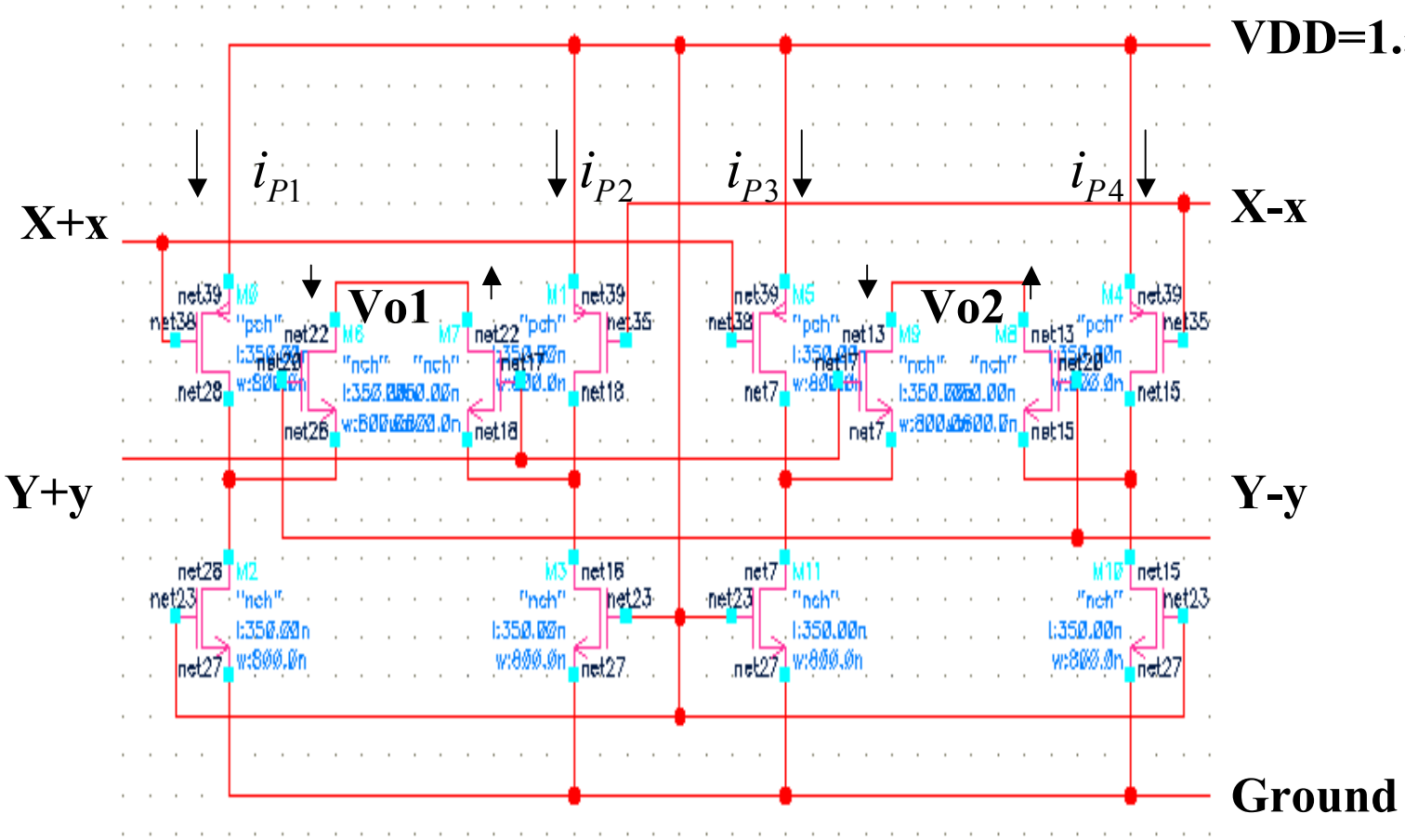


Fig. 12. Second Multiplier Structure

14. Theoretical Analysis of Second structure

For the PMOS transistors, we have:

$$i_{P1} = \frac{1}{2} K_P (V_{DD} - X - x - |V_{THP}|)^2 [1 + \lambda (V_{DD} - V_{P1})] \qquad i_{P2} = \frac{1}{2} K_P (V_{DD} - X + x - |V_{THP}|)^2 [1 + \lambda (V_{DD} - V_{P2})]$$

$$i_{P3} = \frac{1}{2} K_P (V_{DD} - X - x - |V_{THP}|)^2 [1 + \lambda (V_{DD} - V_{P3})] \qquad i_{P4} = \frac{1}{2} K_P (V_{DD} - X + x - |V_{THP}|)^2 [1 + \lambda (V_{DD} - V_{P4})]$$

For the transistors N1-N4, we have:

$$i_1 = K_N [(Y + y - V_{P1} - V_{THN})(V_{O1} - V_{P1}) - \frac{1}{2}(V_{O1} - V_{P1})^2] \qquad i_2 = K_N [(Y - y - V_{O1} - V_{THN})(V_{P2} - V_{O1}) - \frac{1}{2}(V_{P2} - V_{O1})^2]$$

$$i_3 = K_N [(Y - y - V_{P3} - V_{THN})(V_{O2} - V_{P3}) - \frac{1}{2}(V_{O2} - V_{P3})^2] \qquad i_4 = K_N [(Y + y - V_{O2} - V_{THN})(V_{P4} - V_{O2}) - \frac{1}{2}(V_{P4} - V_{O2})^2]$$

And also, we realized that:

$$i_{P1} + i_1 = i_{M1} \qquad i_{P2} - i_2 = i_{M2} \qquad i_{P3} + i_3 = i_{M3} \qquad i_{P4} - i_4 = i_{M4}$$

14. Theoretical Analysis of Second structure

The transistors M1-M4 can be considered as the resistors with resistance approximately equal to $R_{ON} \approx \frac{1}{K_M (V_{DD} - V_{THN})}$

Solving the equations above with $i_1 = i_2$ $i_3 = i_4$ gives the following approximate result:

$$V_{O1} - V_{O2} \propto \frac{K_N K_M}{K_P} xy$$

which is a multiplication of two input signals, x and y

The bias conditions is

$V_P - |V_{THP}| \le X \pm x \le V_{DD} - |V_{THP}|$ For P1-P4

$Y \pm y \ge V_O + V_{THN}$ For N1-N4

15. Linearity Analysis of Second structure

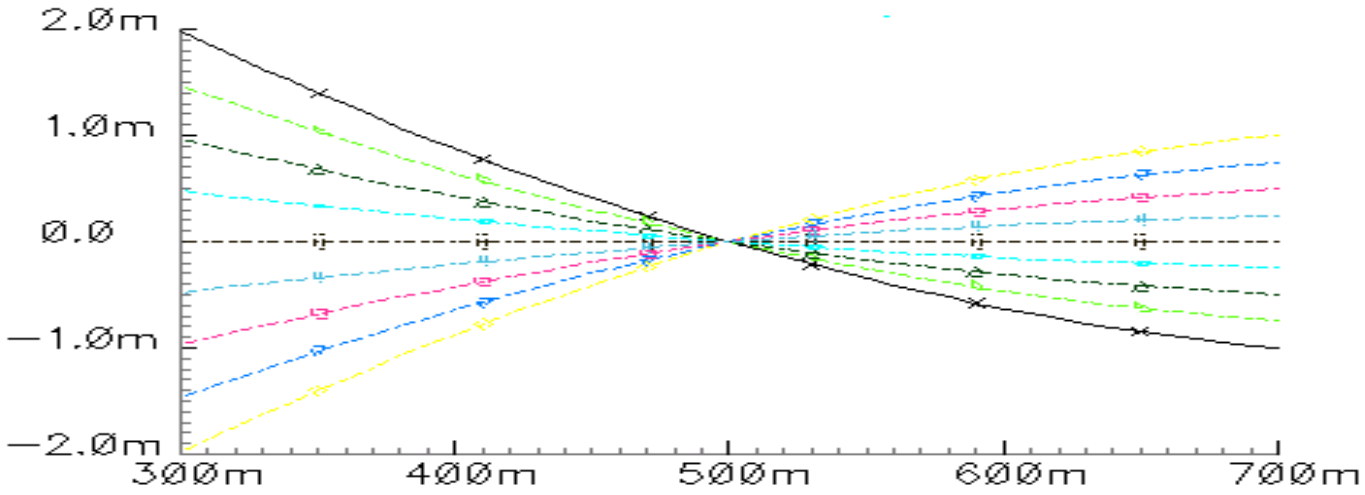


Fig. 13.(a) DC Response for signal x (with body effect)

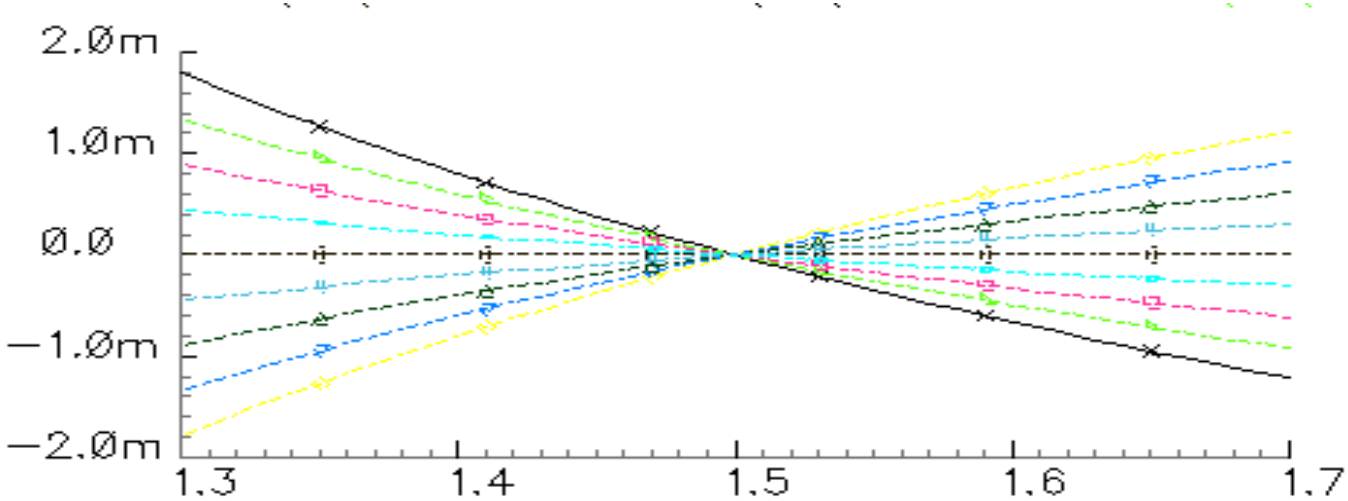


Fig. 13.(b) DC Response for signal y (with body effect)

15. Linearity Analysis of Second structure

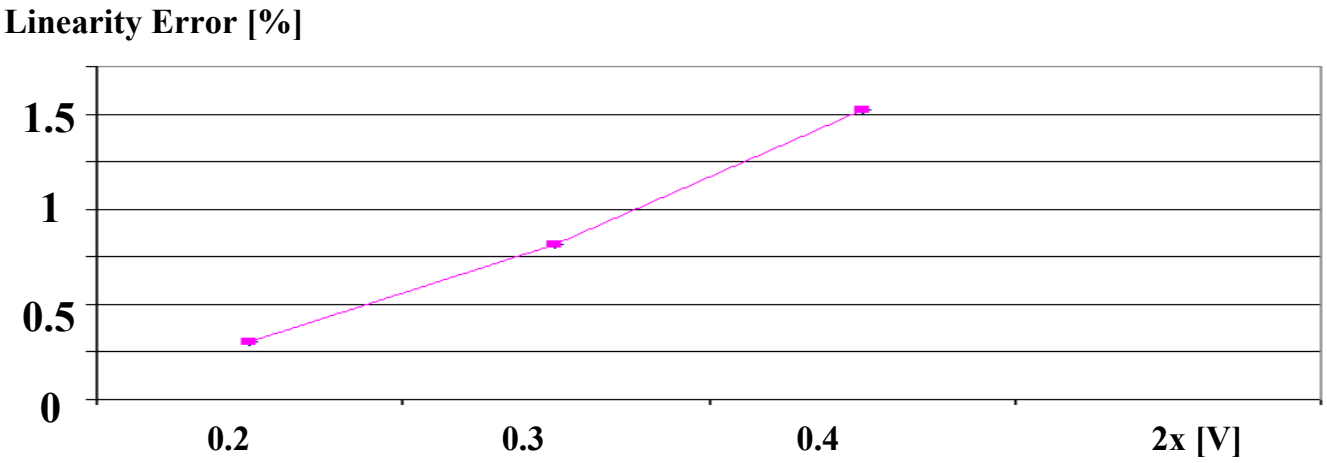


Fig. 14.(a) Linearity Error of signal x with 2y=0.4V (with and without body effect)

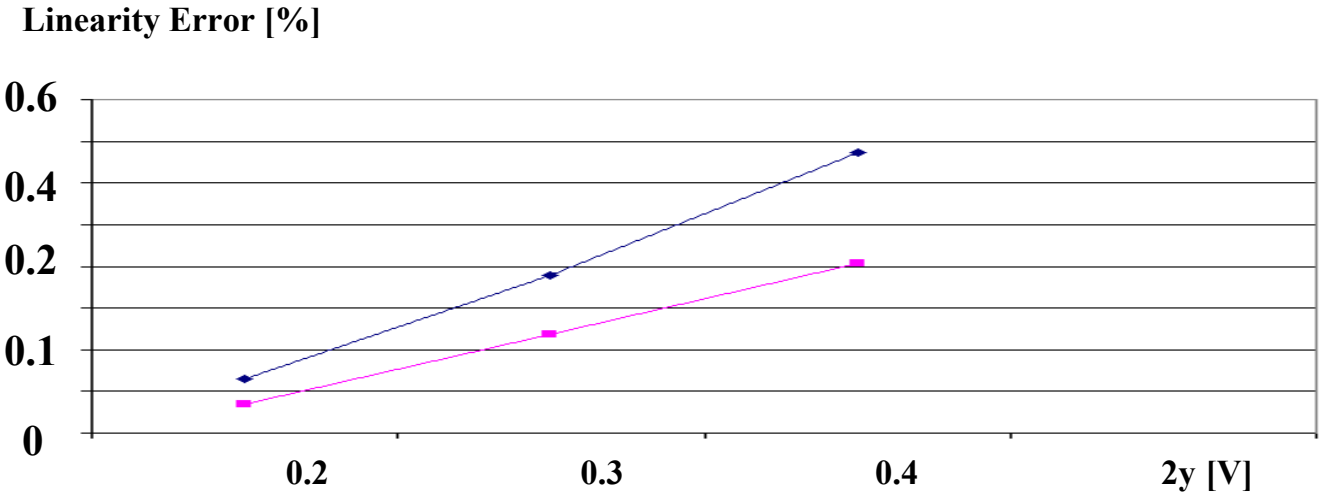


Fig. 14.(b) Linearity Error of signal y with 2x=0.4V (with and without body effect)

16. Power Consumption of Second Structure

Power consumption can be estimated by total current:

$I_{total} = i_{P1} + i_{P2} + i_{P3} + i_{P4}$ Therefore

$$I_{total} = \frac{1}{2}K_P(V_{DD} - X - x - |V_{THP}|)^2[1+\lambda(V_{DD} - V_{P1})] + \frac{1}{2}K_P(V_{DD} - X + x - |V_{THP}|)^2[1+\lambda(V_{DD} - V_{P2})]$$

$$+\frac{1}{2}K_P(V_{DD} - X - x - |V_{THP}|)^2[1+\lambda(V_{DD} - V_{P3})] + \frac{1}{2}K_P(V_{DD} - X + x - |V_{THP}|)^2[1+\lambda(V_{DD} - V_{P4})]$$

Approximately, we have $I_{total} \propto 2K_P[(V_{DD} - X - |V_{THP}|)^2 + x^2]$

We see that the power dissipation has nothing to do with the signal y and DC bias Y for transistors N1-N4.

16. Power Consumption of Second Structure

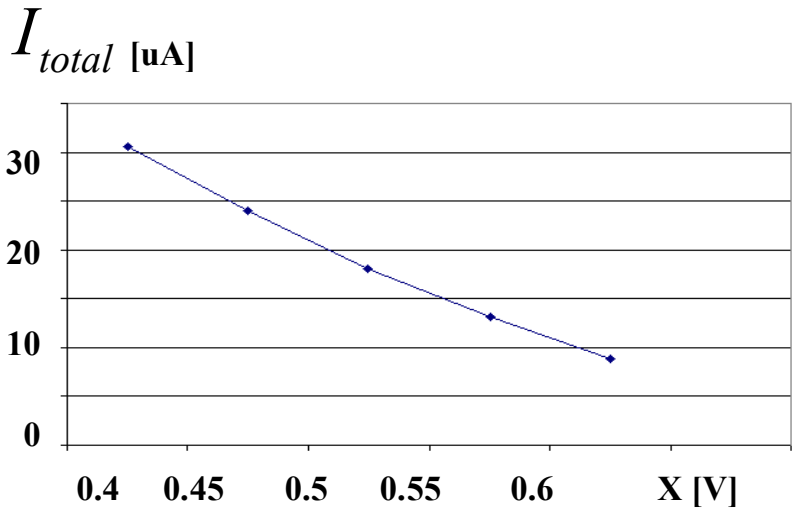


Fig. 15.(a) Total Current Versus X

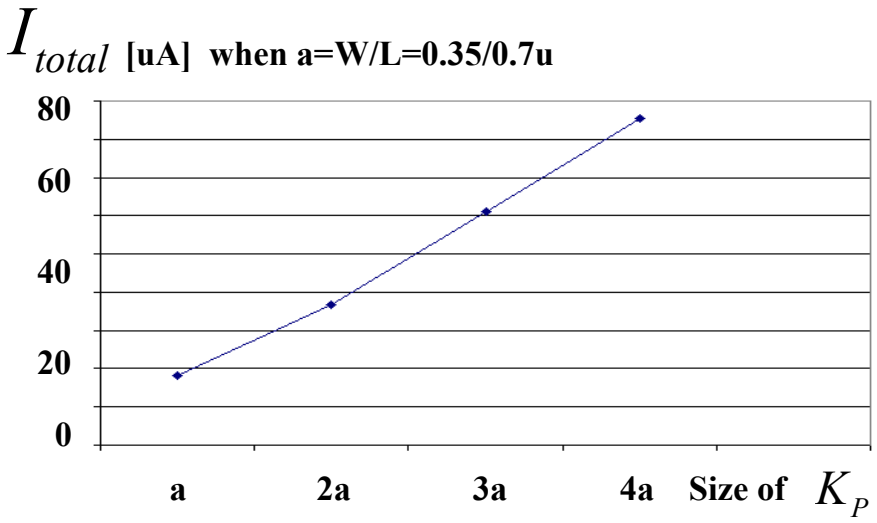


Fig. 15.(b) Total Current Versus K_P

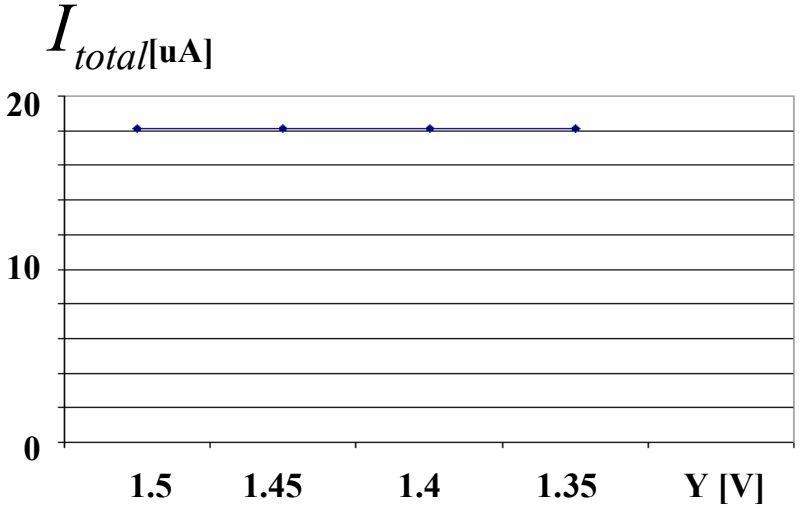


Fig. 15.(c) Total Current Versus Y

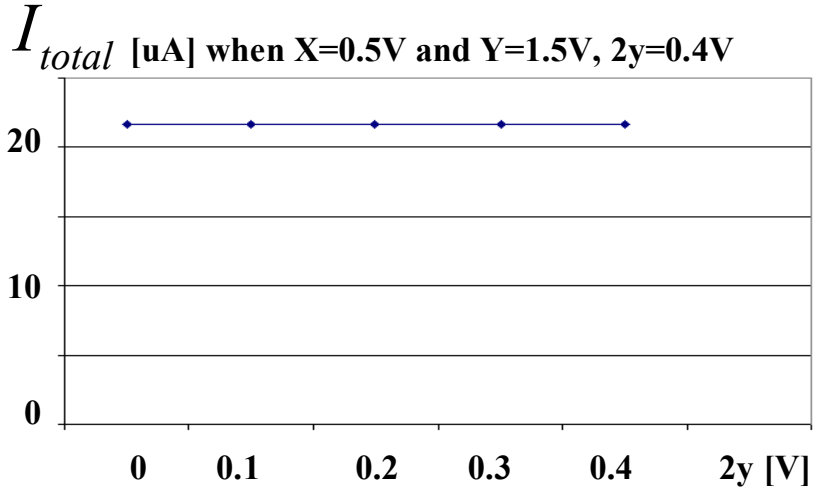


Fig. 15.(d) Total Current Versus 2y

17. Noise Analysis of Second Structure

The total output noise of Fig. 11 is given by

$$\overline{i_{n;o}^2} = 8\overline{i_{n;lin}^2} + 4\overline{i_{n;sat}^2} = 16kTg_{ds1}df + 16kTg_{ds2}df + \frac{32}{3}kTg_m df$$ where

$$g_{ds1} = K_N(Y - V_O - V_{THN})$$

$$g_{ds2} = K_M(V_{DD} - V_P - V_{THN})$$

$$g_m = K_P(V_{DD} - X - |V_{THP}|)$$

Then, the total input noise would be

$$\overline{v_{n;o}^2} = 8\overline{v_{n;lin}^2} + 4\overline{v_{n;sat}^2} \propto 16kT\frac{K_P^2}{K_M^2}df + 16kT\frac{K_P^2}{K_N^2}df + \frac{32}{3}kT\frac{K_P^4}{K_M^2K_N^2}df$$

This suggests that K_M , K_N should be increased and K_P should be decreased to improve the noise performance

17. Noise Analysis of Second Structure

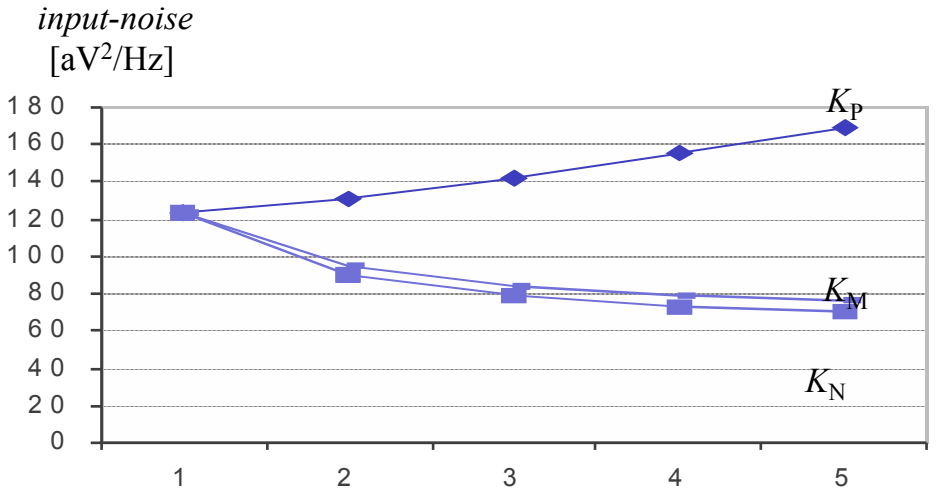


Fig 16(a) The input-referred noise voltage of Fig. 2 versus K_P, K_M and K_N

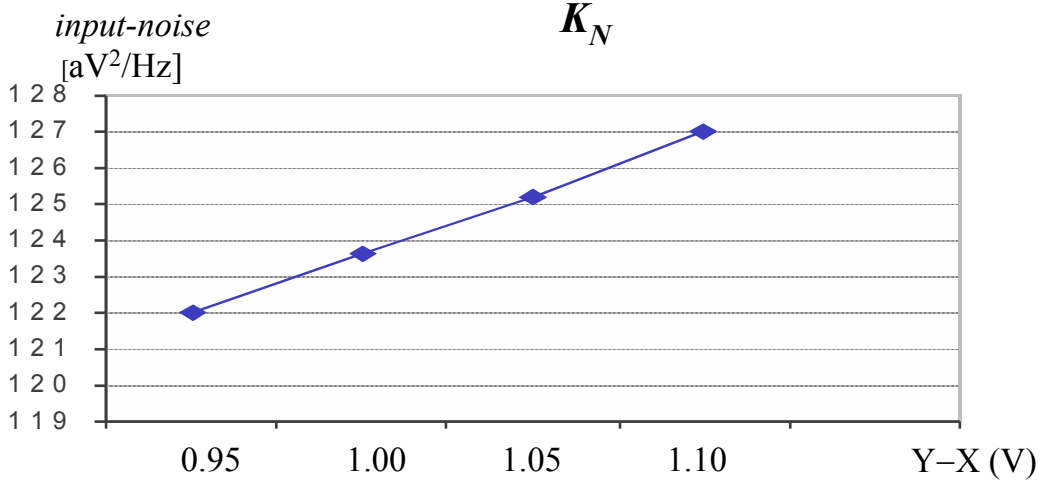


Fig 16(b) The input-referred noise voltage of Fig. 2 versus Y-X

18. Layout of Second Multiplier structure

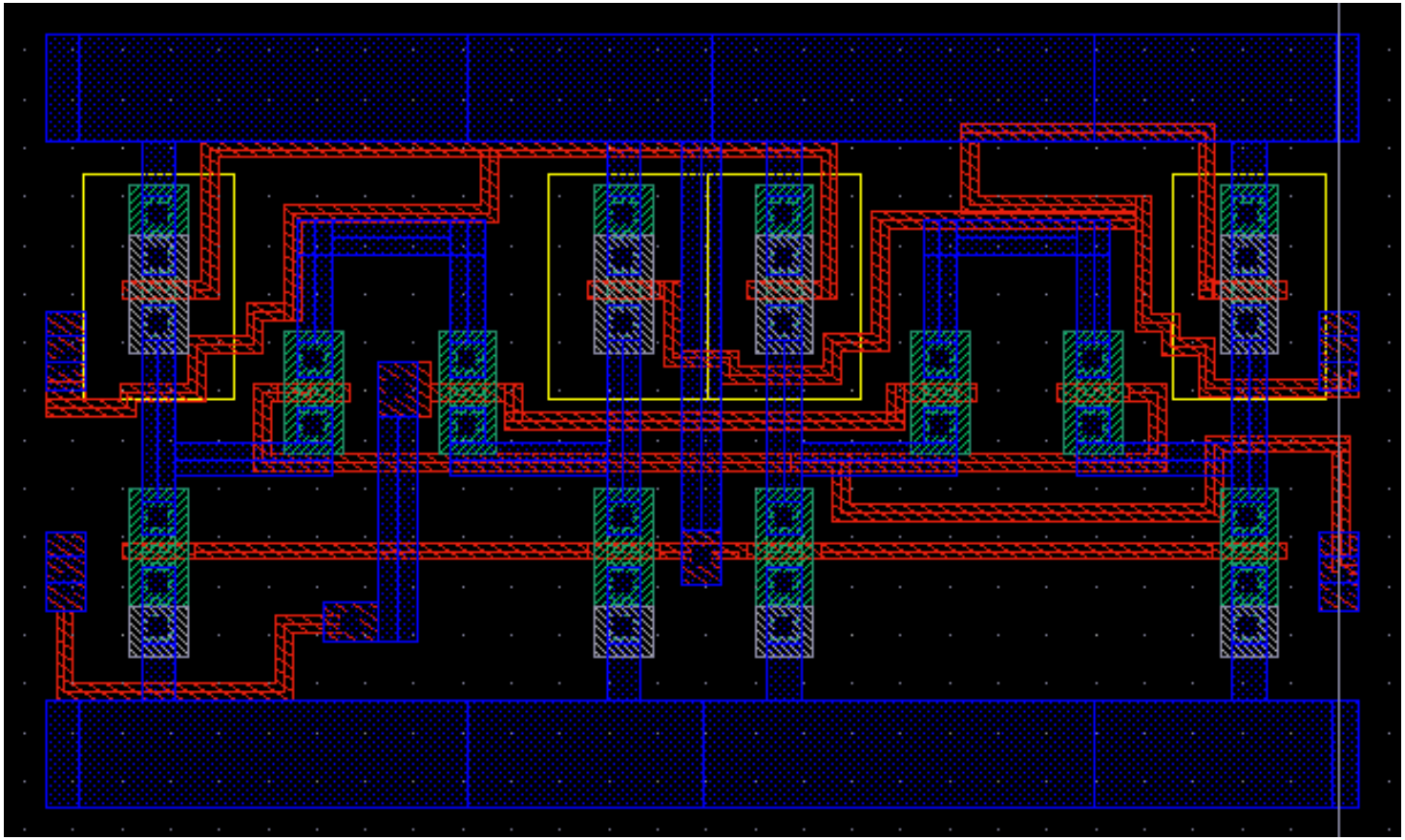


Fig. 17 Layout of our second multiplier structure

19. Extracted Structure

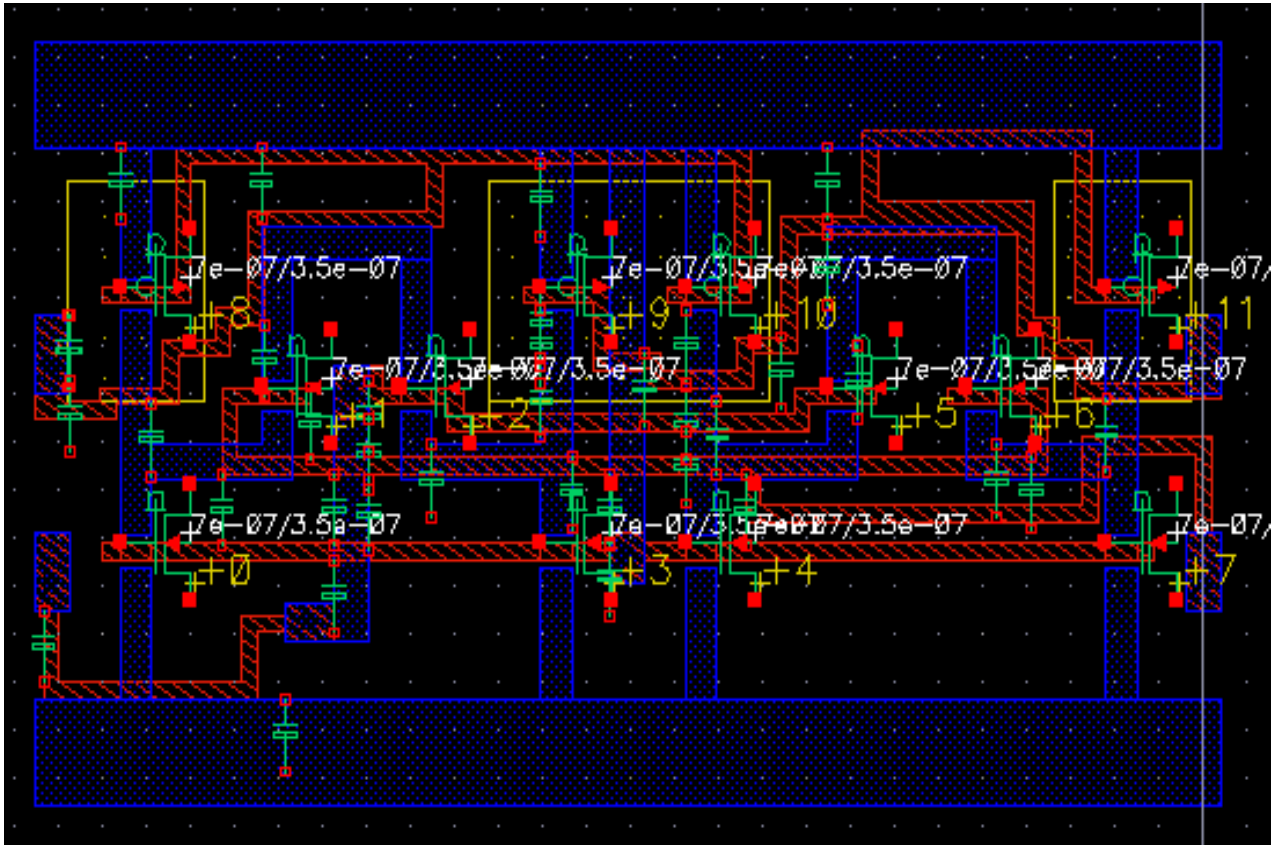


Fig. 18 Extracted Second Multiplier Structure

20. Comparison before and after layout

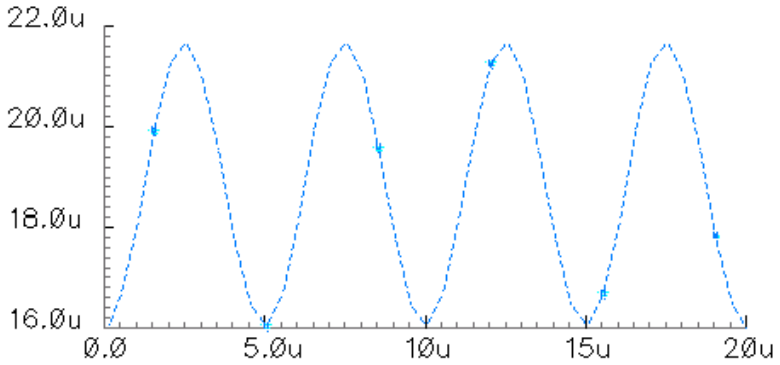


Fig. 19 (a) The comparison of total current before and after layout

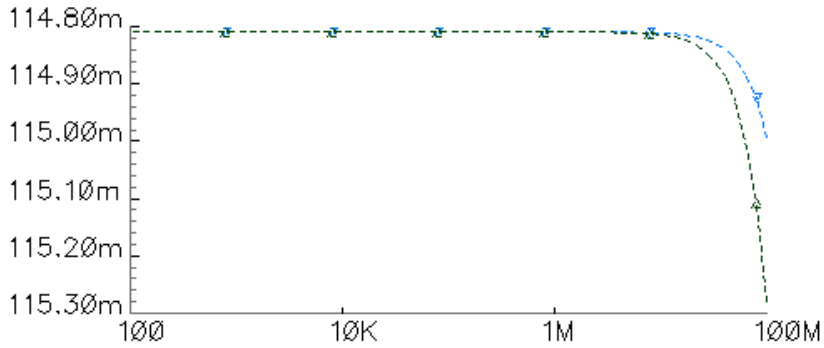


Fig. 19 (b) The comparison of AC response before and after layout

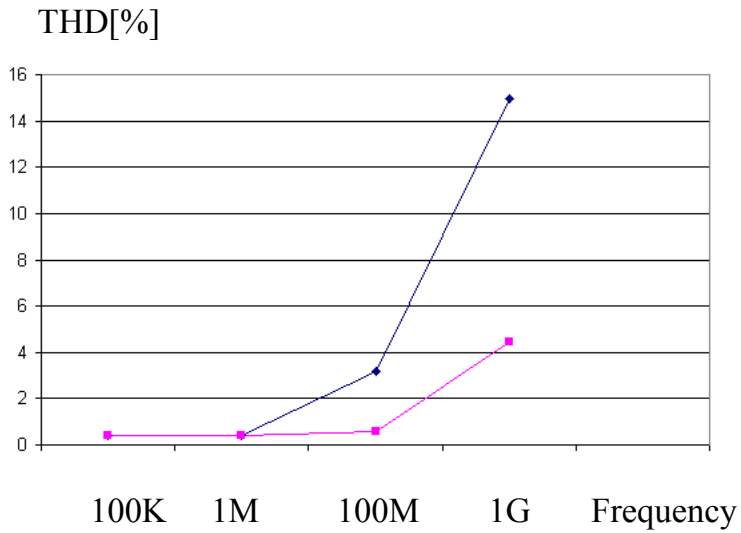


Fig. 19 (c) The comparison of THD for signal 2x=0.4V before and after layout with frequency

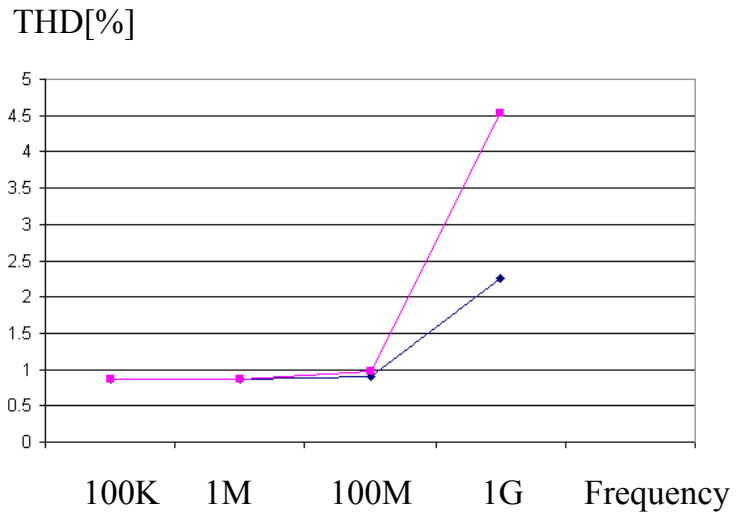


Fig. 19 (d) The comparison of THD for signal 2y=0.4V before and after layout with frequency

21. Most recommended structure by [3]

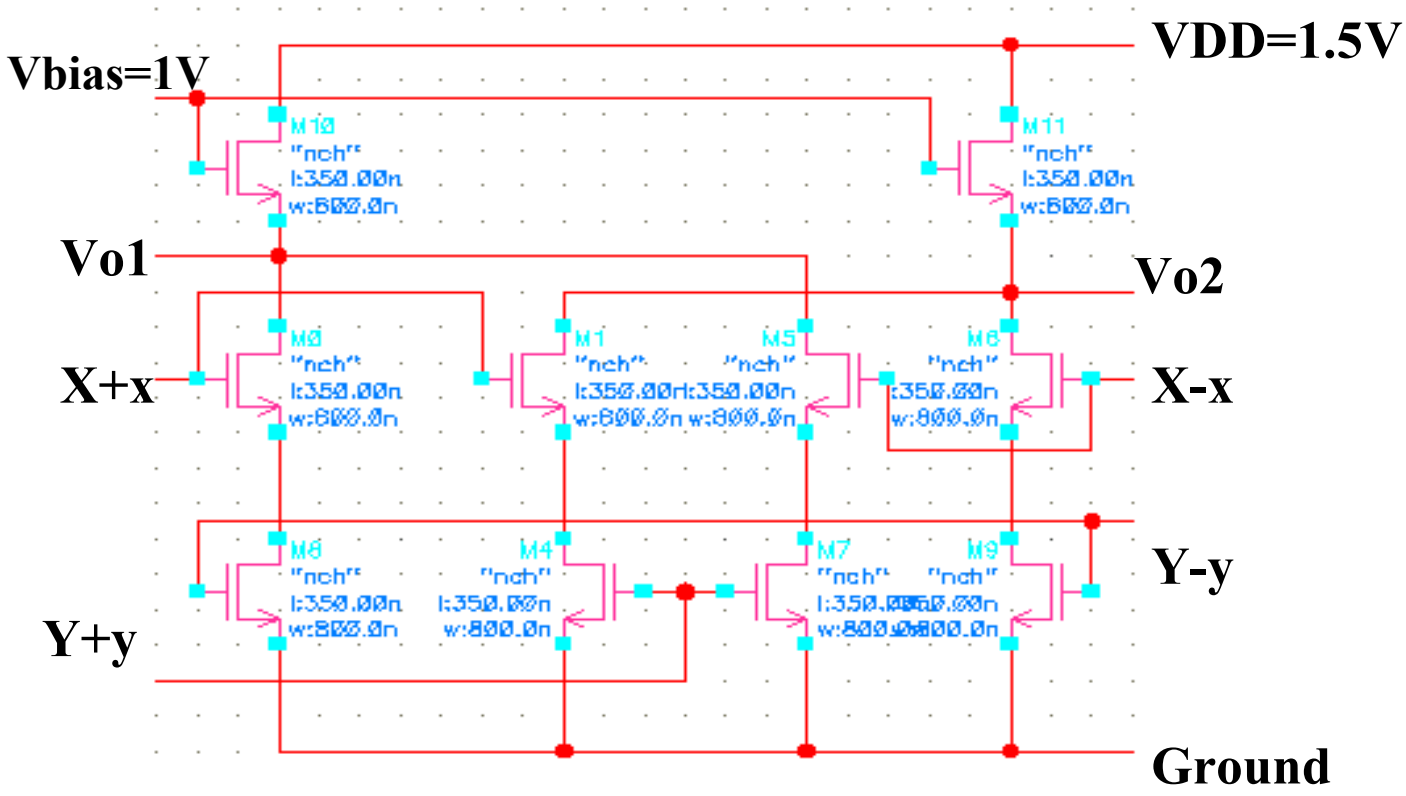


Fig. 20 The most recommended multiplier structure by[2]

22. Comparison of Three Structures

	Our First Structure	Our Second Structure	Most Recommended by[2]
Power Consumption	22.65u	27.15u	68.31u
Estimated Area	12u*12u	27u*16u	
Linearity Error of x	0.8%	1.5%	3.3%
Linearity Error of y	2.6%	0.48%	0.9%
THD of x	0.43%	0.4%	0.4%

22. Comparison of Three Structures

	Our First Structure	Our Second Structure	Most Recommended by[2]
THD of y	0.51%	0.8%	1.1%
Noise	76a	128a	109a
Band width	2G	80M	80M
Number of Transistors	6	12	10
Technology	CMOS 0.35	CMOS 0.35	CMOS 0.35

Conclusion

- By Biasing the transistors in the linear region and decrease the drain-source voltage, we could get low current while at the same time, keeping a relatively wider input range. This is the basic idea of our low power design.
- We try to use transistors as few as possible if we could satisfy the other performance metrics in order to get less area fabrication.
- Body effect is an important second-order effect which we have to consider for good linearity.
- In the layout level, for the differential structure, try to make involved parasite resistors and capacitors symmetric.
- Post-layout simulation is important for performance verification.
- Our two structures have less power consumption compared with the most recommended structure in [2] while keeping other performance good.

Reference

[1] K. Bult and H. Wallinga, "A four-quadrant analog multiplier," *IEEE Journal of Solid-State Circuits*, vol. Sc-21, no.3, pp. 430-435, June 1986.

[2] G. Han and E. Sanchez-Sinencio, "CMOS transconductance multipliers: A tutorial," *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing*, vol. 45, no. 12, pp. 1550-1563, December 1998.

[3] B. Razavi, "Design of analog CMOS integrated circuits," *New York: McGraw-Hill, 2001*.

[4] K.R. Laker and W. M. C. Sansen, "Design of Analog Integrated Circuits and Systems," *New York: McGraw-Hill, 1994*.

And another about 70 papers in the Literature survey.

The papers I have submitted to the conferences:

- **A Low Power and Lower Noise CMOS Analog Multiplier**
- **A Low Power CMOS Analog Multiplier**

Thanks a lot!